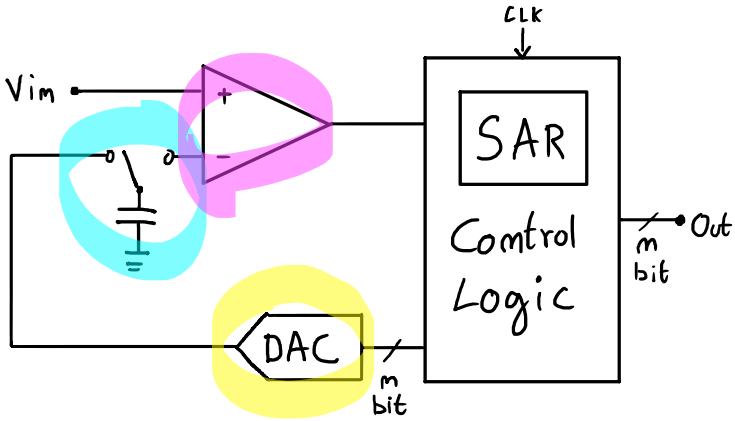
1a) Describe the most important characteristics, number of bits, and typical frequency of conversion of a successive approximation voltmeter helping with a diagram of the voltmeter.



12 to 18 bits

500kHz to 10MHz

A SAR ADC (or voltemeter) works by successively comparing the input voltage to a given voltage, generate in a binary search style.

To do so a DAC is needed to generate the voltage. To keep the generated voltage a S&H block is needed, and to compare it to the input a comparator is needed.

So Vin is compared firstly to half the dinamic range of the ADC, if higher the first bit is set to 1. If lower the first bit is instead set to 0. And so on, increasing or decreasing the generated voltage to try to match the input voltage the best it can.

1b) Is it possible to realize a SAR voltmeter through a pipeline architecture? Then, draw the block diagram of a SAR voltmeter with 16 bit realized with an ADC of 8 bit.

No. SAR → One bit at the time during several comparisons.

Pipeline → bits by stage, with a latency

1c) Is it possible to realize a flash converter through a pipelined architecture?

Also NO. Flash → All bits at the same time

Pipeline → bits by stage, with a latency

1d) An A/D converter with 16 bit, frequency of conversion 500 kS/s, with internal noise with variance $\sigma^2 = 4 \times 10^{-8}\ V^2$, a dynamic from 0V to 3V. Calculate the number of equivalent bits of the converter.

$m = 16\,bit$

$f_s = 500\,kHz$

$\sigma_{im}^2 = 4 \times 10^{-8}\ V^2$

$D = 0 - 3V$

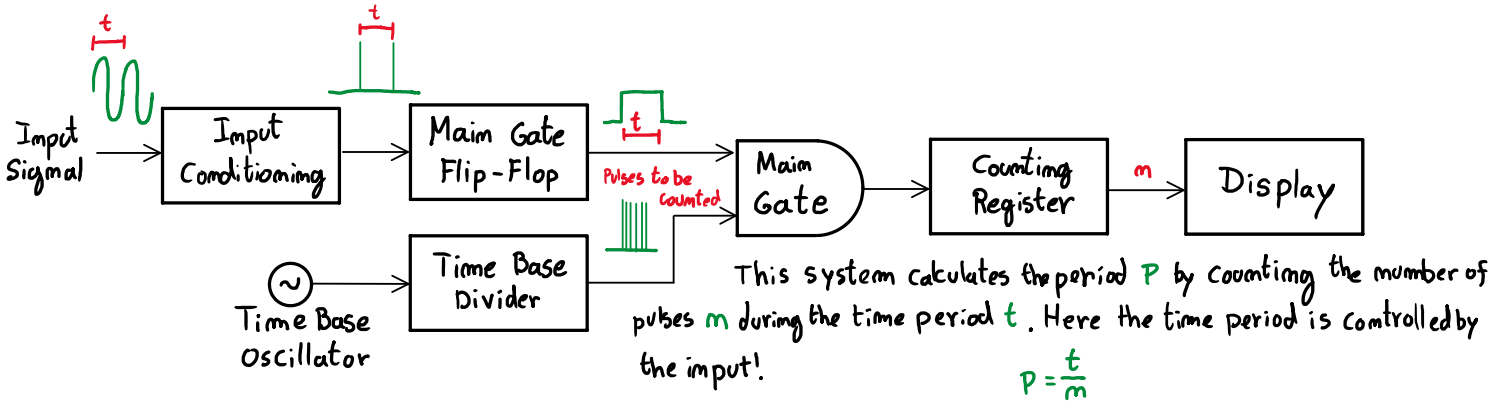
$$\Delta V = \frac{D}{2^m}$$

$$\sigma_q^2 = \frac{\Delta V^2}{12} = \frac{D^2}{2^{2m}12} \approx 175 \times 10^{-12}\ V^2$$

$$ENOB = m_e = m - \frac{1}{2}\log_2\left(\frac{\sigma_c^2}{\sigma_q^2}\right) \Rightarrow m_e = m - \frac{1}{2}\log_2\left(\frac{\sigma_q^2 + \sigma_{im}^2}{\sigma_q^2}\right) \approx 12\,bit$$

$$\sigma_c^2 = \sigma_q^2 + \sigma_{im}^2 + \sigma_{Ext}^2$$

2a) Briefly describe briefly, helping with a block diagram, a time interval measurement in a counter.



2b) Write in boxes below how many counts are displayed on a counter in frequency measurement mode with an opening of 100 ms to measure a sinusoidal frequency of 10 kHz

$t = 100\,ms \rightsquigarrow f_{res} = 10\,Hz$

0	0	0	1	0	0	0

$\times 10\,Hz$

$f_{im} = 10\,kHz$

$\frac{f_{im}}{f_{res}} = 1000$

2c) What it is displayed measuring the same frequency of 10 kHz in period configuration using an internal clock of 5 MHz?

0	0	0	0	5	0	0

$\times 200\,ms$

$T_{res} = \frac{1}{f_{clk}} = 200\,ms$

$T_{im} = \frac{1}{f_{im}} = 100\,\mu s$

$\frac{T_{im}}{T_{res}} = 500$

The internal temperature of a processor varies proportionally with the velocity of the fan mounted on it. If we set the following velocities expressed in rounds per minute (RPM) you measure these temperatures:

V (RPM)	1250	1500	1750	2000	2250
T (°C)	55	48	44	42	39

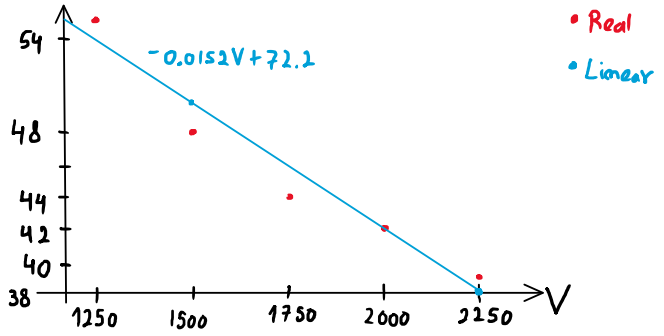
3a) **find empirically the relationship between velocity and temperature**

Linear regression $T = \alpha V + \beta$

$$\alpha = \frac{m\sum_{i=1}^{m} T_i V_i - \sum_{i=1}^{m} T_i \sum_{i=1}^{m} V_i}{m\sum_{i=1}^{m} V_i^2 - \left(\sum_{i=1}^{m} V_i\right)^2} = -0.0152 \qquad \beta = \frac{\sum_{i=1}^{m} T_i - \alpha \sum_{i=1}^{m} V_i}{m} = 72.2$$

$$T = -0.0152V + 72.2$$

3b) Plot on a graph the experimental points and the obtained regression curve.



3c) Knowing that the maximum velocity of the fan is 2250 rpm, how much is the temperature of the processor at 20% of it's maximum velocity?

$V_{Max} = 2250 \rightarrow 0.2\, V_{Max} = 450 \quad \Rightarrow T = -0.0152 \cdot 450 + 72.2 = 65.36\,^{\circ}C$

With a DAQ board we want to acquire the following signals:

V1: a square wave, duty cycle 50%, period 1 ms, amplitude 0-5V, with 20 points per period

V2: a sine wave alternated at 25 kHz with peak amplitude of 1V

4a) What is the correct modality of acquisition and the number of channels necessary to acquire the two signals?

Single mode and 2 channels

4b) Calculate the maximum frequency of the internal ADC in order to acquire the two signals.

V_1 : $f_S = 20 \cdot \frac{1}{1 \cdot 10^{-3}} = 20\ kHz$

V_2 : $f_S = 2 \cdot 25 \times 10^3 = 50\ kHz$

$\Rightarrow f_{ADC} = m_{ch} \times Max\{f_S\} = 2 \times 50\ kHz = 100\ kHz$

4c) If the board has an ADC with dynamic from -5V to +5V, and 14 bits, what will be the resolution of the ADC?

$D = \pm 5\ V$

$m = 14$

$\Delta V = \frac{D}{2^m} = \frac{10}{2^{14}} \approx 610\ \mu V = 0.61\ mV$