1a) Draw the circuit diagram of a data acquisition board (DAQ), which is the component that allows you to acquire more than a signal with a single ADC? The acquisition of multiple signals takes place simultaneously? Justify your answers.

1b) Indicate what are the minimum features (input mode, the ADC frequency, individual channel gain, number of bits) must have a DAQ, inside which there is present an amplifier with gain $G = 0.5, 1, 10, 100$ and an A/D with dynamic ± 3 V, in order to acquire the following signals at the same time:

V_1 analog signal with a maximum bandwidth of 20 kHz, maximum amplitude: 100 mV peak-to-peak, zero mean value, for which you want to appreciate details with resolution better than 0.1 mV.

V_2 square wave with analog levels 0 V and 3 V, at a frequency of 500 Hz, of which you must acquire at least 50 samples per period.

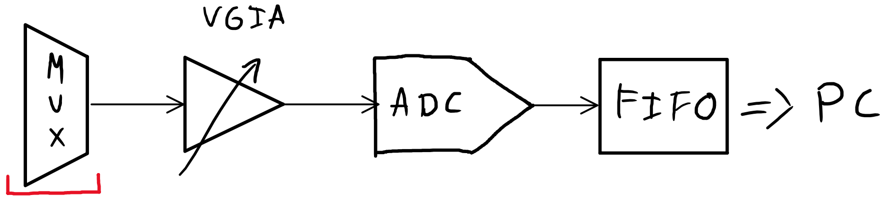
V_3 temperature signal coming from a thermocouple, with sensitivity of 50 μV/K, used to measure a temperature of an oven at 500 ° C, with a resolution of at least 0.35 °C.

V_4 Signal from an absolute pressure sensor, with sensitivity of 15 mV/kPa placed at 10 meters below the sea level (1 atm = 101.325 kPa), which measures the pressure with resolution $\Delta V_4 = 1$ mV.

1c) What kind of analog to digital converter is probably used in DAQ, as suitable for this measurement? If you need to acquire an additional signal V_5 with analogue bandwidth: 10 MHz and amplitude which varies between ± 2 V which type of converter (indicate the architecture between those you know) would need to use in a new DAQ board, which acquires all the five signals?

The acquisition of the signals is done sequentially by sweeping all the channels one by one, using the MUX.

1a)



Controls the number of channels

1b) $D_{ADC} = \pm 3V$ $G = \{0.5; 1; 10; 100\}$ $D_{DAQ} = \{\pm 6; \pm 3; \pm 0.3; \pm 0.03\}$ V

V_1: $Bw = 20kHz$, $D = \pm 50$ mV, $\Delta V_{min} = 0.1$ mV

V_2: $D = 3V$, $f = 500 Hz$, 50 samples per period

V_3: $S = 50 \mu V/K$, $T_{oven} = 500°C$, $\Delta C_{min} = 0.35°C$

V_4: $S = 15 mV/kPa$, $d = 10m$, $\Delta V_{min} = 1mV$

Input mode: V_3 (the thermocouple) requires differential input mode.
So we need 8 channels 4 pairs of 2 channels in differential mode

Frequency: V_3 and V_4 don't present any requirements regarding the sampling freq.

$V_1 \Rightarrow f_{s1_{min}} = 2 Bw = 40 kHz$

$V_2 \Rightarrow f_{s2_{min}} = 50 \cdot f = 25 kHz$

$f_{sDAQ} = 4 \cdot Max\{f_{s_{min}}\} = 160 kHz$ //

Channel Gain: $V_1 \Rightarrow G_1 = 10$

$V_2 \Rightarrow G_2 = 1$

V_3 $\Delta T = T_{oven} - T_{Ref} = 500 - 25 = 475$

$D = S \cdot \Delta T = 23.75 mV \Rightarrow G_3 = 100$

V_4 $P_{Sea} = \rho \cdot g \cdot d \cong 1 atm$

$P_{sensor} = 1 atm + P_{Sea} = 2 atm$

$D = P_{sensor} \cdot S = 3.04 V \Rightarrow G_4 = 0.5$

Number of bits: No limitation on V_2

$V_1 \Rightarrow \Delta V = 0.1 mV$

$m = \log_2\left(\frac{D_{DAQ}}{\Delta V}\right) = 12.5 \Rightarrow 13 bit$

$V_3 \Rightarrow \Delta V = 0.35 \cdot 50 \mu V = 17.5 \mu V$

$m = \log_2\left(\frac{D_{DAQ}}{\Delta V}\right) = 11.7 \Rightarrow 12 bit$

$V_4 \Rightarrow \Delta V = 1 mV$

$m = \log_2\left(\frac{D_{DAQ}}{\Delta V}\right) = 13.5 \Rightarrow 14 bit$

8 channels in diff mode
$m = 14 bit$
$f_s = 160 kHz$

1c) $m = 14$
$f_s = 160\ kHz$ → A SAR or Sigma Delta would be enough!

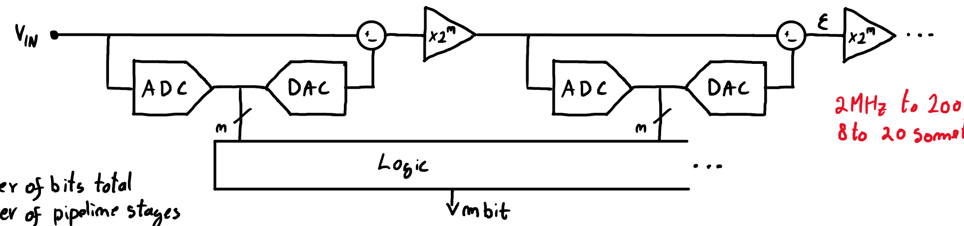
V_5: $BW = 10\ MHz$
$D = \pm 2$
$\Rightarrow f_s' = 5 \cdot 2 \cdot 10\ MHz = 100\ MHz$

$f_s = 100\ MHz$
$m = 14$
} → Pipeline!

2a) Briefly describe, with the help of the instrument diagram block scheme, the principle of operation of a *pipeline* voltmeter / converter without recursion (feedback).
2b) For this type of voltmeters write the typical values of resolution and speed.
2c) Draw and explain how works a pipeline voltmeter with recursion.
2d) What is the dependance between the speed of the measurement, circuit complexity and the number of bits of the pipeline converter? Then compare these features with corresponding of a *flash* voltmeter.
2e) Write the formula of equivalent bits and then explain its meaning comparing it with that of the bit computing.

This ADC works by converting the input voltage to a low number of bits and then comparing the result of that conversion with the input voltage. This will produce an error which will be amplified and then will be passed to the next stage of the ADC which will do the same thing

2a)

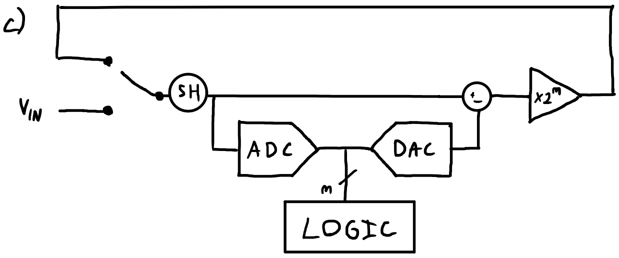


2MHz to 200 MHz
8 to 20 something bits

$m = m \times p$

m: number of bits total
p: number of pipeline stages
m: number of bits of a stage

2c)



Equal to the other one but instead of having several stages, it uses only one stage and used feedback to always use that same stage.

2d) Conversion Speed = T_{stage}
Time due to pipeline = $p \times T_{stage}$

The number of bits doesnt affect the conversion time, however it increases the pipeline time! Note that adding more bits is just a question of adding more stages, so the increase in complexity is linear to the amount of bits. This will be limited by the accuracy is limited by the exponential amplifier

Flash: On a flash, the increase in the number of bits will also not affect the conversion time. However increasing the number of bits in this architecture implies an increase in complexity that is exponential, since you need to effectively double the number of comparators.

2e) $$m_e = M - \frac{1}{2}\log_2\left(1 + \frac{\sigma^2_{A/D} + \sigma^2_{Ext}}{\sigma^2_Q}\right)$$

The equivalent number of bits is the number of bits that in an ADC carry information. All the bits lost are still on the output, but they are only quantizing noise, therefore not being effective.

3a) Describe briefly, with the aid of a block diagram, how it works the time interval measurement in an electronic counter.

3b) Write in the boxes below what is currently displayed (how many counts makes the instrument) on the display of a counter in the **frequency** measurement mode with an opening time of 100 ms when the frequency of 10 kHz is measured:

0	0	0	1	0	0	0

×10

$t_{op} = 100$ ms, $t_{im} = 1/10$ kHz, $m = \frac{t_{op}}{t_{im}} = 1000$, $f_{scale} = 1/t_{op} = 10$ Hz

and what is shown on the display by measuring the same frequency of 10 kHz using a 5 MHz clock with counter in **period** measurement mode:

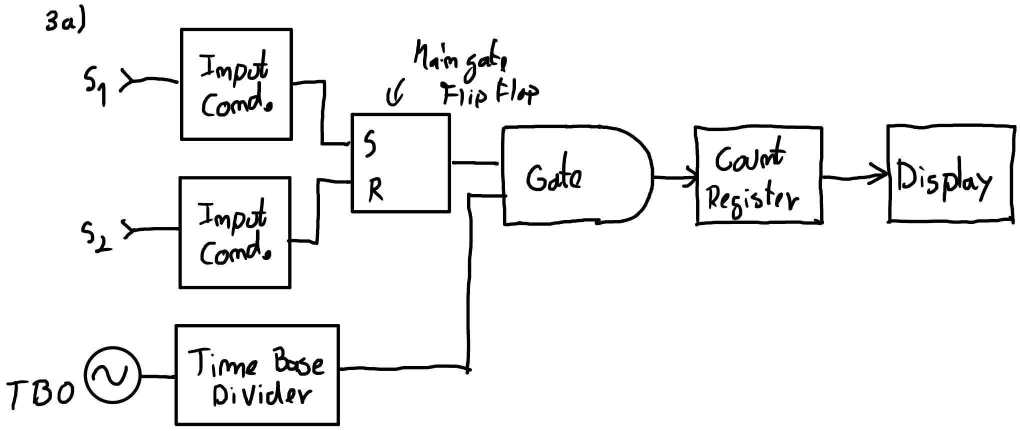
0	0	0	0	5	0	0

×0.2 µs

$t_{op} = 1/10$ kHz, $t_{im} = 1/5$ MHz, $m = \frac{t_{op}}{t_{im}} = 500$

In time interval two external signals are used to control the main gate. One first starts the opening time, the other ends it. This is controled by a flip-flop. During the opening time the count registers counts the number of pulses generated by the time base oscilator.

3a)



It is wanted to measure the differential efficiency of a semiconductor laser (the slope of the emitted power curve vs. the current that feeds). To do this are accomplished 6 measures the power emitted by the laser to vary the injected current, which give the following results:

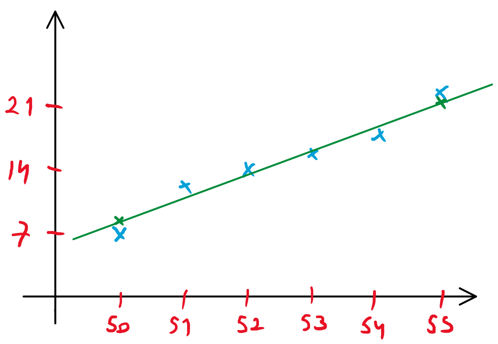
Current (mA)	50	51	52	53	54	55
Power (mW)	7.02	12.21	13.96	15.53	17.74	23.07

4a) Draw in a graph the measured data points.

4b) Calculate, using the linear regression procedure, the efficiency differential value (mW/mA) and the laser threshold (the current for which the laser starts to emit power).

4c) Show, by drawing it, on the same graph the regression curve obtained.

4 a)



$m = 2.81$

$b = -132.$