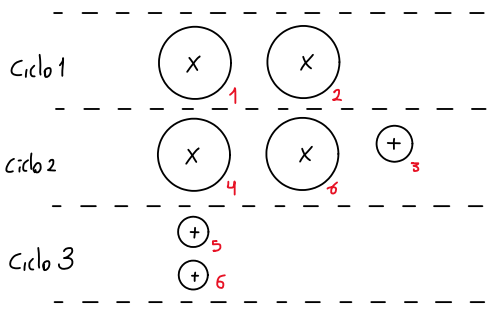
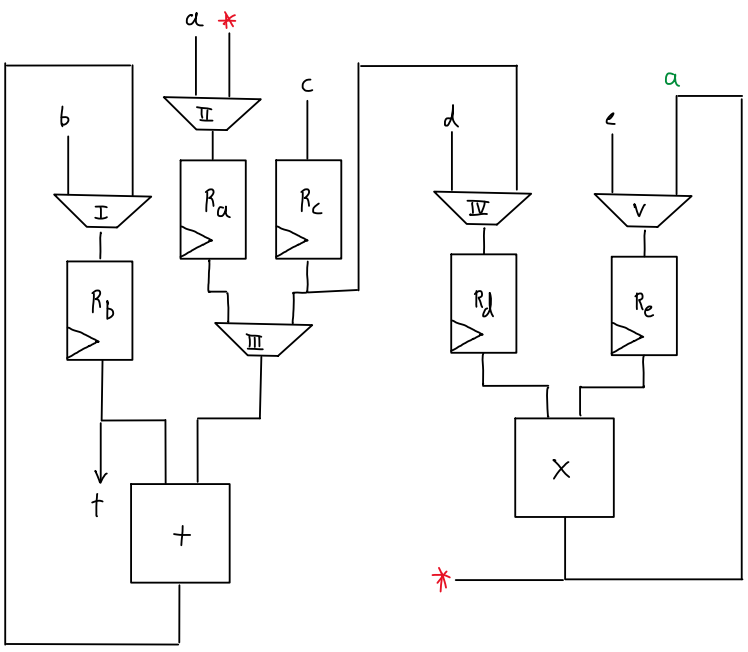
1.

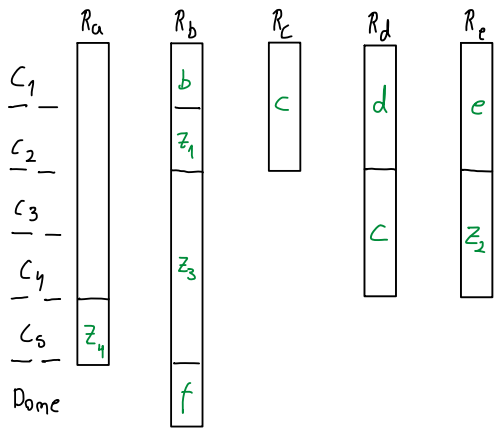
	Op	CritPath	Dep
1	a x b	4	— ✓
2	c x d	4	— ✓
3	1 + 2	3	1,2 ✓
4	e x f	3	— ✓
5	3 + 4	2	3,4 ✓
6	g x h	2	— ✓
7	5 + 6	1	5,6 ✓

$t_{clk} = 2\,ns \Rightarrow$ CritPath para 1 mul



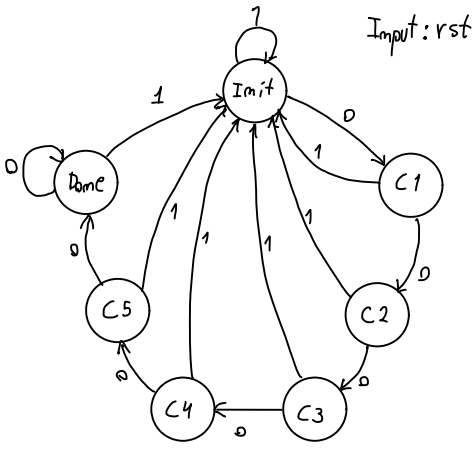
2.





$z_1 = b + c \quad z_3 = a + z_1 \quad f = z_4 + z_3$

$z_2 = d \times e \quad z_4 = c \times z_2$



	En_a	En_b	En_c	En_d	En_e	Sel I	Sel II	Sel III	Sel IV	Sel V	Estado
Imit	1	1	1	1	1	0	0	—	0	0	11000
C_1	0	1	0	0	0	1	—	1	—	—	10110
C_2	—	1	—	1	1	1	—	0	1	1	11010
C_3	—	0	—	0	0	—	—	—	—	—	00010
C_4	1	0	—	—	—	—	1	—	—	—	01010
C_5	—	1	—	—	—	1	—	0	—	—	10010
Dome	—	0	—	—	—	—	—	—	—	—	01011
	b_3	b_4	b_3			b_1		b_2	b_1		↳ Valid

$Area = 5 \times MUX2{:}1 + 5 \times Reg + Add + Mul = 266$

$t_{CLK} = Max \begin{cases} t_{pFF} + t_{SET} + t_{Mul} + t_{MUX} = 20\,ms \\ t_{pFF} + t_{SET} + t_{add} + 2t_{MUX} = 14\,ms \end{cases}$

Latencia : $5 \times 20\,ms = 100\,ms$

4 a)

$S = A - D \Rightarrow$ A: Q 12.4, B: Q 2.14 $\rightsquigarrow$ S: $Q_{13.14}$

$M = 4.5 \times S \Rightarrow$ 4.5: $Q_{4.1}$, S: $Q_{13.14}$ $\rightsquigarrow$ M: 16.15 (Ou podemos fazer $4S + \frac{S}{2}$)

$Y = M + C \Rightarrow$ M: $Q_{16.15}$, C: $Q_{30.2}$ $\rightsquigarrow Y: Q_{31.15}$

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity madda is
	Port (
		a : in std_logic_vector (15 downto 0);
		d : in std_logic_vector (15 downto 0);
		c : in std_logic_vector (31 downto 0);
		yi : out std_logic_vector ( 30 downto 0);
		yf : out std_logic_vector ( 14 downto 0 )
	);
end madda;

architecture behavioral of madda is
signal as, ds : signed(15 downto 0);
signal cs : signed(31 downto 0);
-- internal signals
signal s : signed( 26 downto 0 );
signal m : signed( 30 downto 0 );
signal y : signed( 45 downto 0 );
signal fourdotfive : signed( 4 downto 0);

signal aAux, dAux : signed(25 downto 0);
signal cAux : signed(44 downto 0);

begin
as <= signed(a);
ds <= signed(d);
cs <= signed(c);
fourdotfive <= 01001;

aAux <= as & "0000000000";
dAux  <= (ad(1)=>(15 downto 6)) & ad;
cAux <= cs & "0000000000000";

-- arithmetic operations

s <= aAux - dAux ;
m <= fourdotfive * s;
y <= cAux * resize(m, length'cAux);

yi <= y(45 downto 15);
yf <= y(14 downto 0);

Begin Process
If (clk'event and clk = '1') then
	# Colocar aqui os seguinte sinais
	a,d,c,s, m, y
end
End;



end;
```

c)

A - D:
Pre Adder de 25 bits $\Rightarrow$ Precisamos de 2 DSP para cascading
Ou usamos uma alu!

4.5 S:
Mult 25 bits x 18 bits $\Rightarrow$ 2 DSP para cascading

M + C:
Precisa 1 ALU

$\Rightarrow$ 2 DSP's !!

S $t_{clk} = t_{P_{FF_{Max}}} + t_{P_{Log_{Max}}} + t_{SET} = 4 + 2 + 10 = 16\,ns$

b) $\delta = -3\,ns$

$t'_{clk} = t_{clk} - \delta = 19\,ns$ WNS = 25 − 19 = 6 ns

c) $t_{HOLD} + \delta < t_{Min}$ $1 < t_{Min} - \delta \Leftrightarrow 1 < 3 - (-3) + 4 \Leftrightarrow 7 < 10$

WHS = 10 − 1 = 9 ns