RF CMOS Fundamentals

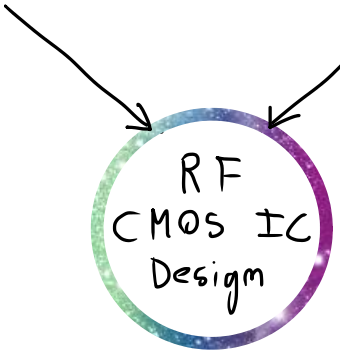
HF Design

HF

GaAs IC
Semi-isolated Substrate
Bottom GND plane
Tuned (Bandpass) Circuits
S - Parameters
Transmission Lines
Model w/Pparasitics

LF

Silicon IC
Conductive Substrate
Guard-Rings
Lowpass Circuits
Y/Z - Parameters
Lumped elements
Post-Layout Parasitics



- Integrated monolithic circuits:
  - Components are monolithic integrated on the same substrate and interconnected with metal tracks;
  - Higher coupling between components and with substrate;
  - High coupling between close interconnects;
  - Guard-rings;
  - Reduced size and usually packaged.

- Discrete circuits:
  - Individual packaged components mounted on a PCB;
  - Reduced coupling between components;
  - Possible coupling between close interconnects;
  - Large size.

- Differences between LF and HF design:
  - HF circuit topologies can be different and simpler than LF ones.
  - Components models have more parasitic effects that were not important at LF.
  - Mandatory and very important to create HF ground nodes/planes clean of AC perturbations.
  - LF circuit theory still valid.

- Distributed effects (DE):
  - When signal frequency is high enough and wavelength (λ=c/f) comparable with circuit or components sizes, distributed behavior appears.
  - PCB boards and large size components can present DE. Long interconnects became transmission lines (TL) caring incident and reflected waves.

If $\lambda_s >> L$: $Z(x) = Z_L$

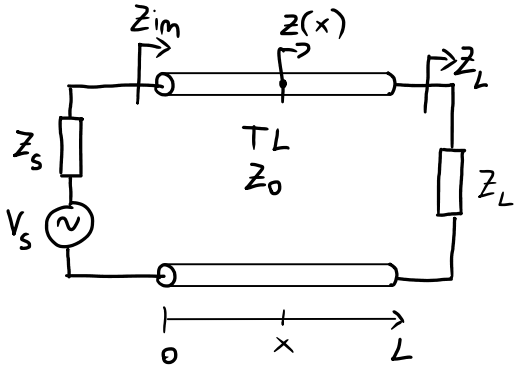
$V(x)$ and $I(x)$ have constant phase and amplitude

No DE!

If $\lambda_s < L$: $Z(x), V(x), I(x)$ can vary along the TL

DE present!

To avoid this $\rightsquigarrow Z_0 \approx R_0$ and $R_s = R_L = R_0$ (Matching)

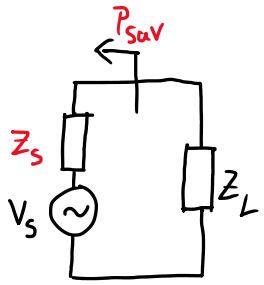


- For the circuit zones where DE is important:
  - Passives like C and L can be replaced by TL which have a better behavior.
  - Power rather than voltage (v) or current (i) is more appropriated to use because v and i magnitudes vary along a TL. Δ
  - Concepts of impedance matching for maximum power transfer and reflection coefficients must be applied.
  - Smith chart is still a useful graphical tool, in paper format or included in some CAD tools.

- Conclusion: In the same circuit/system LF and HF regions can coexist. The presence of DE is related with local frequency and physical size. Usually inside chips these effects only appear for extremely high frequencies due to the chip very small size. Still, the PCB where the chip is mounted probably will present DE on RF signal interconnects.

Power Gains

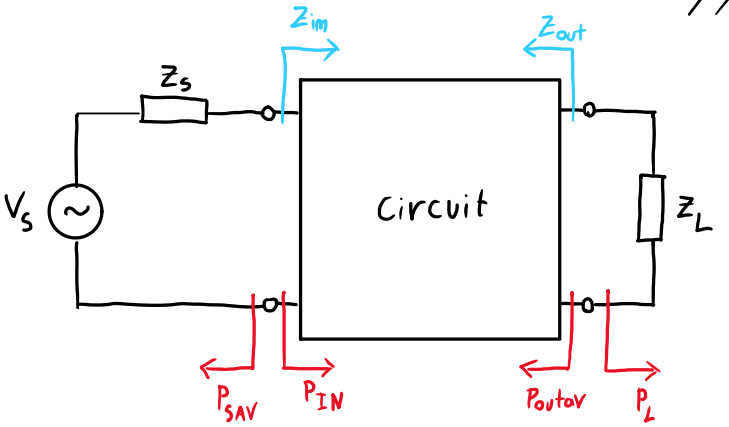
P_{SAV} & Z_S defines the source!



As noted in Δ, it's better to work in power.

So, a SOURCE is defined by it's available power and internal impedance.

Available Power: P_{SAV} is the power a source delivers to a load with value $Z_L = Z_S^*$



P_{SAV} – Available power from the source

P_{IN} – Power delivered to input

P_{outSAV} – Available power from the output

P_L – Power delivered to load

Operating Power Gain – $G_P = \frac{P_L}{P_{IN}}$ ⇒ accounts for output mismatch

Available Power Gain – $G_A = \frac{P_{outSAV}}{P_{SAV}}$ ⇒ accounts for input mismatch

Transducer Power Gain – $G_T = \frac{P_L}{P_{SAV}}$ ⇒ accounts for input and output mismatch

Particular cases:

Input Match Output Mismatch ⇒ $Z_{in} = Z_S^* \Rightarrow P_{IN} = P_{SAV} \Rightarrow G_T = G_P < G_A$

Input Mismatch Output Match ⇒ $Z_{out} = Z_L^* \Rightarrow P_L = P_{outSAV} \Rightarrow G_T = G_A < G_P$

Input Match Output Match ⇒ $Z_{out} = Z_L^*$ and $Z_{in} = Z_S^* \Rightarrow G_T = G_P = G_A$

Notes: S-Parameters

$Z_S = Z_L = R_0 = 50\Omega \Rightarrow \rho_S = \rho_L = 0$:

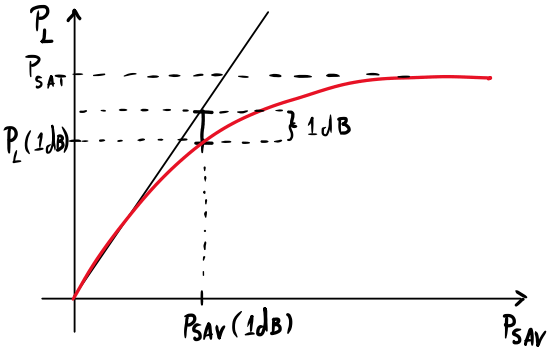
$G_T = |S_{21}|^2$ $\quad G_A = \frac{|S_{21}|^2}{1-|S_{22}|^2}$

$G_P = \frac{|S_{21}|^2}{1-|S_{11}|^2}$ $\quad \rho_{in} = S_{11}$ $\quad \rho_{out} = S_{22}$

Nonlinear Behavior

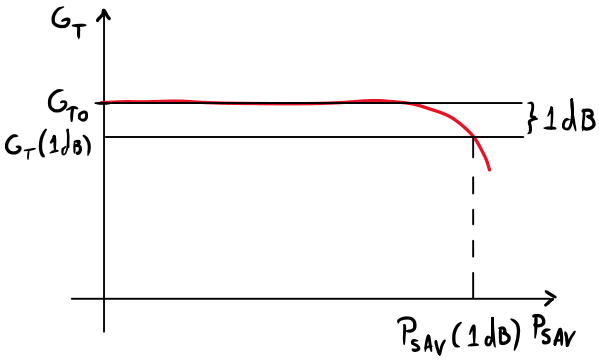
* 1dB Compression Point (CP1)

The point where gain value reduction from linear gain is 1dB defines the CP1



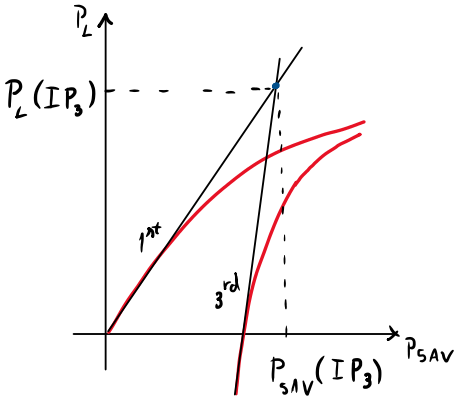
⇐ Input specified

Output specified ⇒



* Third Order Intermodulation intercept point (IP3)

Point at which the 3rd order power curve at the input intercepts the 1st order power curve

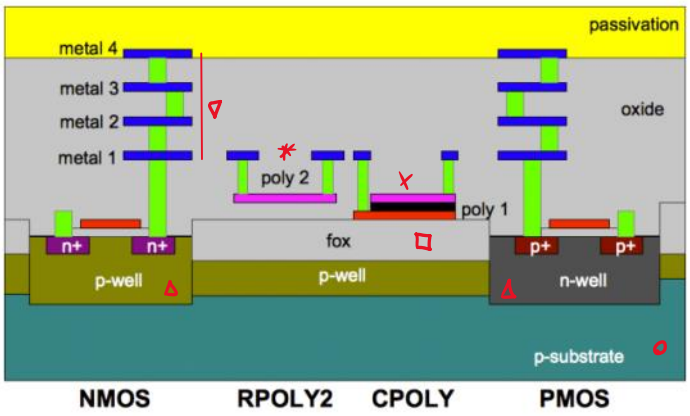


The distance between the 2 curves is the 3rd-order intermodulation distortion (IM3)

$$IM_3 = \frac{P_L(2\omega_1 - \omega_2) \rightarrow 3^{rd}\ order}{P_L(\omega_1) \rightarrow 1^{st}\ order}$$

CMOS Technology

Typical structure:



Main features:

- P - substrate o
- Twin - well △
- LOCOS □
- 4 Metal layers ▽
- Poly 1-2 Capacitor ×
- Poly 2 Resistance *

Guard Rings

Guard-rings are used to make electrical connections of p-wells or n-wells to a fixed potential.

The n-well guard-rings are connected to the circuit most positive bias source (VDD). The p-well guard-ring are connected to the circuit most negative bias source (VSS).

Guard-rings are usually placed around individual devices (RF case) or group of devices (LF case), connecting their wells to a fixed potential.

Passives can reside on a p or n well, depending on the manufacturer options.

Although the guard-ring makes a well connection, this connection is usually referred as to substrate (or bulk, or body) connection. The bottom p-substrate has no direct electrical connection.

Guard-rings have their typical ring rectangular shape when placed around device(s). For connecting well regions without devices other shapes can be used.

Advantages:

- Reverse bias between n-well and p-well junctions.
- Isolate current flow (crosstalk) across those junctions.
- Isolate devices on the same well region from outside.
- Improve substrate equipotentiality.

Disadvantages:

- Increase devices parasitic coupling to well.
- Increases layout area and connections complexity.

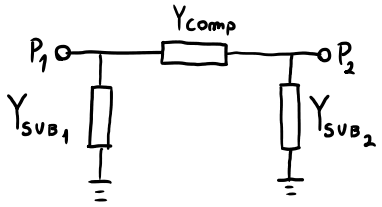
Passive compoments

- Overview:

RF PI Model for passive compoments like R, C and L

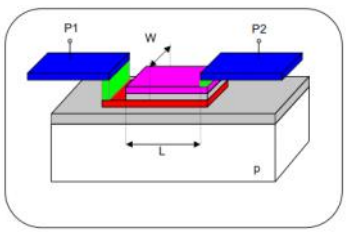
Y_{comp} is the compoment intrimsic model

$Y_{SUB_{1,2}}$ is the compoment parasitic due to the substrate

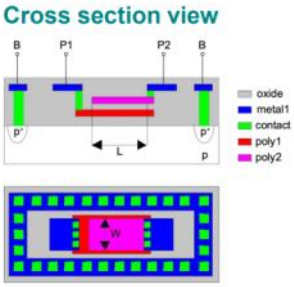


- At LF Y_{comp} dominates, the device is near ideal.
- At RF $Y_{SUB_{1,2}}$ can affect!
- If P_1 or P_2 is grounded => Only one Y_{SUB} is in parallel with Y_{comp} => Less intluence!

- CPoly:



Simplified angled view of a cpoly (guard-ring is omitted)



Plan view - layout

➢ Uses the capacitance between poly1 and poly2 layers.

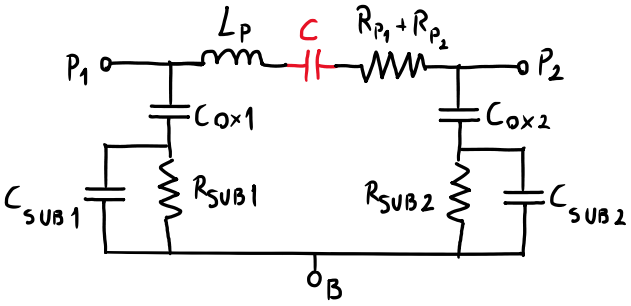
➢ It is a linear capacitance => advantage for non-linear applications.

➢ Capacitor plates are not metal but polysilicon => plate losses. With a careful layout these can be minimized.

➢ Usually, it is a large area component.

➢ Losses in the substrate are important because poly layers are close to it, especially bottom plate.

➢ MIM and MOM capacitors are better, but only expensive CMOS provide them.



C: Capacitor Value

R_{P_1}: poly1 plate resistance

R_{P_2}: poly2 plate resistance

L_P: parasitic inductance

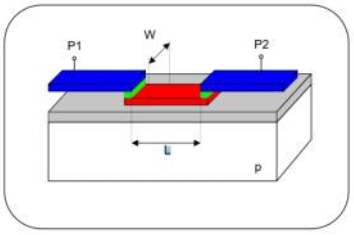
$C_{ox1}, R_{SUB1}, C_{SUB1}$: Coupling between poly1 and substrate. Can be important!

$C_{ox2}, R_{SUB2}, C_{SUB2}$: Coupling between poly2 and substrate. Less important!

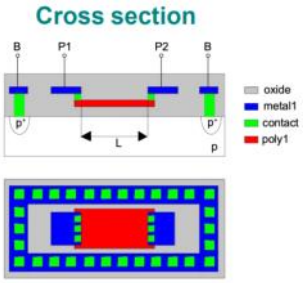
Notes:
The coupling to the substrate depends of the shape and the distance to the guard-ring.

Some manufacturers (like AMS) do not include coupling between P2 and B.

• R Poly



Simplified angled view of a rpoly (guard-ring is omitted)



Plan view - layout

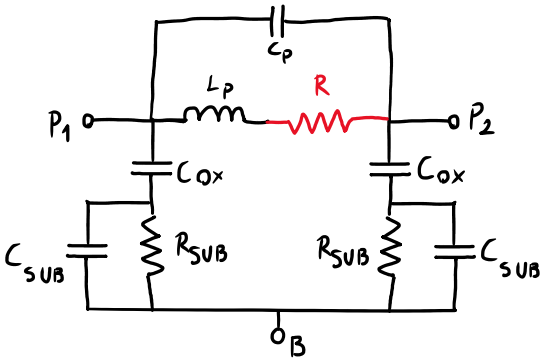
➢ It uses the available poly layers with different resistivities.

➢ It is a linear resistance => advantage for non-linear applications.

➢ Usually with rpoly1 or rpoly2 it is not possible to build high value resistances (R< 1kΩ). For higher values some manufactures made available another polysilicon layer with a higher resistivity value.

➢ Losses in the substrate are important because poly layers are close to it.

➢ Usually a complete symmetric device.



R: Resistance value

C_P: Parasitic capacitance

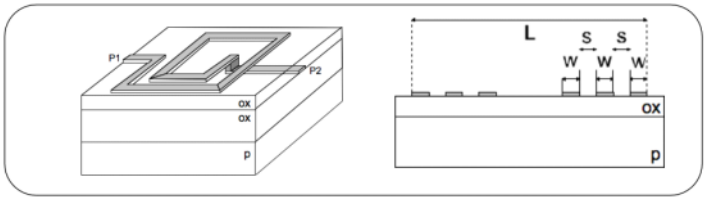
L_P: Parasitic inductance. Less important!

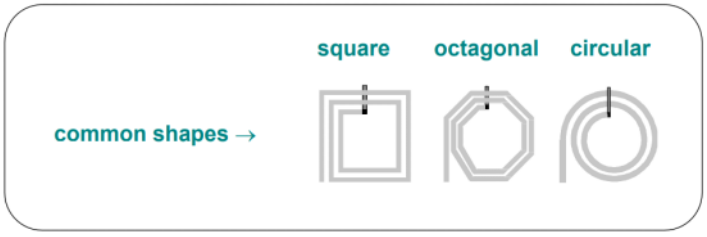
C_{ox}, R_{SUB}, C_{SUB}: Coupling between poly and substrate.

Notes:
The coupling to the substrate depends on the shape and the distance to the guard-ring.

Some manufacturers (like AMS) use the T model topology instead.

• Spiral Inductor





➢ Easily built in a standard low-cost integrated circuit technology without additional steps.

➢ Less occupied area and higher precision L value than an equivalent bondwire solution.

➢ Parasitic effects due to doped substrate and low conductivity metal affects inductor performance => Low Q and self-resonant frequency.

- Metal Losses

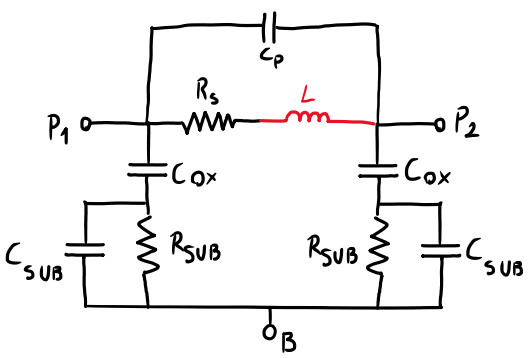
Im DC and LF → Ohmic losses due to metal resistivity ⇝ $R_{LF} = \frac{\rho}{T}\frac{L}{W}$

Im RF → Ohmic losses due to { Skin effect ⇝ $R_{HF} = \frac{R_{LF}}{1 - e^{-\frac{T}{\delta}}}$; $\delta = \sqrt{\frac{2\rho}{\omega\mu}}$; Eddy currents

L - Lenght
W - Width
T - Thickness
ρ - Resistivity
ω - Angular frequency
μ - Permeability

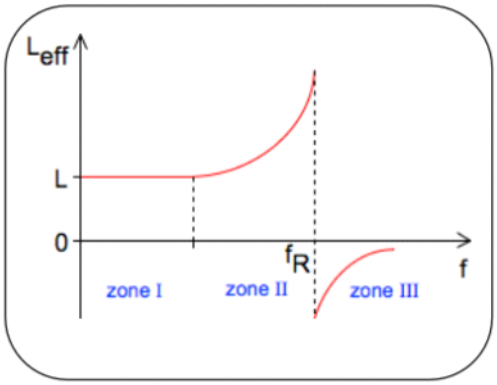
- Substrate Losses

- Ohmic losses due to current flow between spirals and guard rings. This current crosses oxide layer through capacitive coupling. This effect increases with frequency
- Ohmic losses due to current flow between spiral turns through the oxide and substrate. This effect increases with frequency.
- Ohmic losses due to Eddy currents induced in the lossy substrate. This effect also increases with frequency.



L : Spiral inductance.
R_s: Spiral resistance DC and AC.
C_p: Capacitance between spirals.
C_{ox}: Capacitance between spirals and substrate.
R_{SUB}, C_{SUB} : Parasitics of the substrate

- Effective inductance (L_{eff}) and self-resonant frequency (f_R)



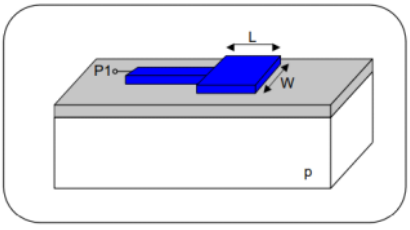
An inductor behavior divides in three regions!

➢ Zone I : Low frequency band where parasitic effects are neglected, and its reactance is purely inductive with a constant Leff. Applications: matching network.

➢ Zone II : Band were, because of the parasitic effects, the inductor Leff increases its reactance and also the . It still has inductive behavior. Applications: bias network where a high not so accurate inductance is required.

➢ Zone III : Band above fR where, due to parasitic effects, the inductor has capacitive behavior. Applications: zone to avoid.

- Pads

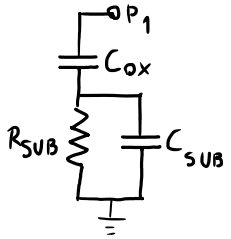


➢ Necessary to apply bias or signals to the circuit, made with the technology top metal and usually has ESD protection.

➢ On encapsulated chips or in chip-on-board (CoB) assemblies they are connected outside with bond-wires.

➢ In on-wafer tests the bias or signals are applied to these pads with special DC or AC probe needles, respectively.

➢ The capacitive coupling to ground is an advantage at DC for a bias pad because it helps to bypass the external bias circuit.



C_{ox}: Capacitance of the pad
R_{SUB}, C_{SUB} : Parasitics of the substrate

Notes:
The coupling to ground depend on the shape and the distance to the guard ring.

This model does not include ESD protection influence.

RF Tuned LNA

Circuits with noise

Circuits with deterministic and noise signals:

The same circuits analysis techniques used for deterministic signals can be used for random noise signals.

Noise signals can be considered incremental due to their usual small rms values. This means that superposition theorem can be used to analyze circuits with noise and deterministic incremental signals.

Due to linear working behavior, noise + deterministic total response can be obtained by adding the noise response plus the deterministic response.

During circuits calculations noise sources can be assumed sinusoidal incremental sources. Total noise response are usually presented in mean-square our rms averages.

If all noise source are uncorrelated, the total noise mean-square response is equal to the sum of all individual noise mean-square responses.

Noise Factor (F)

IEE definition: It is the relation between a two-port input and output SNR obtained with an input thermal noise source at T0=290K (16.8ºC).

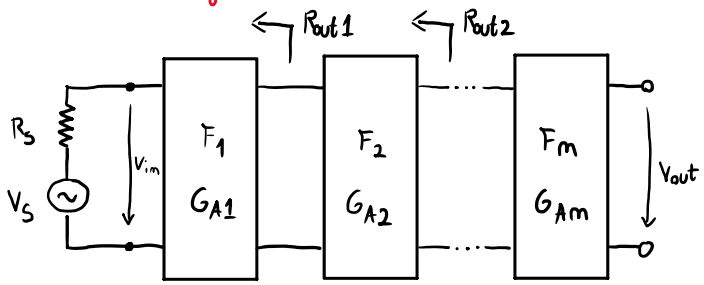
$$F = \frac{\left(\frac{S}{N}\right)_{im}}{\left(\frac{S}{N}\right)_{out}} = \frac{\left(\frac{S}{N}\right)_{SAV}}{\left(\frac{S}{N}\right)_{OUTSAV}} = \frac{S_{SAV}}{S_{OUTSAV}} \cdot \frac{N_{OUTSAV}}{N_{SAV}} = \frac{1}{G_A} \cdot \frac{N_{qAV} + G_A N_{SAV}}{N_{SAV}} = 1 + \frac{N_{qAV}}{G_A N_{SAV}}$$

- N_{qAV} : Internal generated output available noise
- G_A : Available power gain

→ If port is noiseless ($N_{qAV}=0$) → $F=1$ SNR maintains!

→ If port is noisy ($N_{qAV}\neq 0$) → $F>1$ SNR reduces!

Cascaded stages



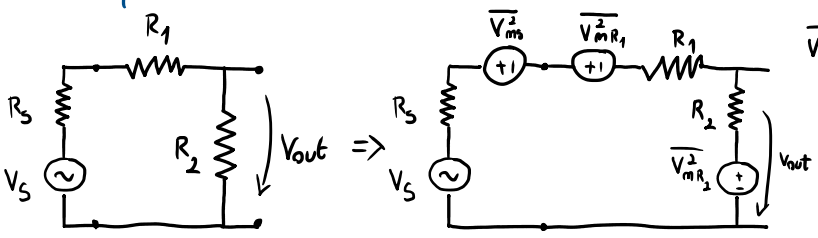
$$F_{tot} = F_1 + \frac{F_2 - 1}{G_{A1}} + \cdots + \frac{F_m - 1}{G_{A1} G_{A2} \cdots G_{A(m-1)}}$$

G_{Ai} - Gain of stage i

F_i - F of stage i

Note: F_1 and G_1 are determinant!

- Example



$$\overline{V_{mx}^2} = 4kTR_x\Delta f$$

$$F = \frac{\overline{V_{nout}^2}}{\overline{V_{ns}^2}} \cdot \frac{1}{A_{VT}^2} = 1 + \frac{R_1}{R_S} + \frac{(R_1 + R_S)^2}{R_2 R_S}$$

If:

$R_2 \to \infty$ Series Res. $F = 1 + \frac{R_1}{R_S}$

$R_1 \to 0$ => Parallel Res. $F = 1 + \frac{R_S}{R_2}$

LNA Stages

Main characteristics:

The Friis equation show us that the first block has the major influence on the total chain noise factor. That is the reason why a low-noise amplifier (LNA) is always the first block in the receiver chain.

The input impedance of a LNA should be matched to the antenna impedance. Usually, its value is 50W. This avoids undesirable standing waves in the transmission line connection to the antenna and also maximizes transducer power gain.

The LNA dynamic range should be high, that is, be able to amplify very weak and very strong signals keeping the system specifications => Care with bias points and transistors size to minimize distortion.

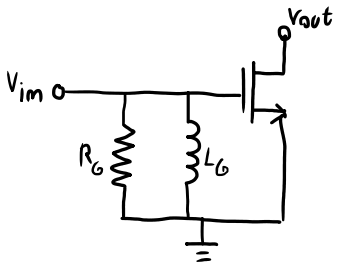
Topologies:

LNA topologies are chosen with the purpose of achieving 50Ω input match, a high power gain, with a noise figure as low as possible.

Circuits can also have single ended and/or differential accesses.

Sometimes cascode topology is used.

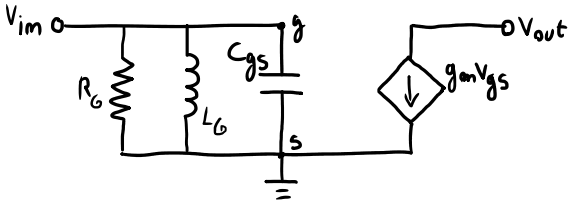
- Commmom source with parallel resomance (CSPR)



$$Y_{im} = sC_{gs} + \frac{1}{sL_G} + \frac{1}{R_G}$$

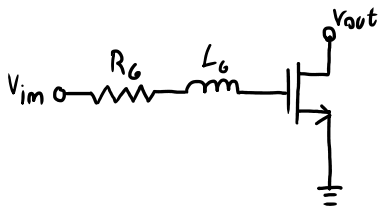
If we have ressomance:

$$Z_{im} = R_G\ !$$



The input impedance of a MOS is almost purely capacitive.
To create the required resistive part for input matching, the RG resistor is added.
Inductor LG tunes with CGS.
Problem: Resistance RG by itself makes F higher than 2 (3dB).

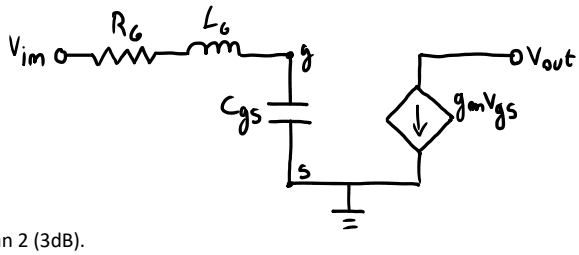
- Commmom source with series resomance (CSSR)



$$Z_{im} = R_G + sL_G + \frac{1}{sC_{gs}}$$

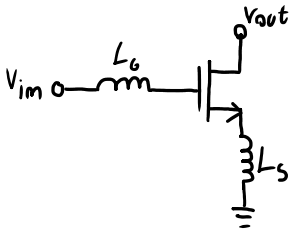
If we have ressomance:

$$Z_{im} = R_G\ !$$

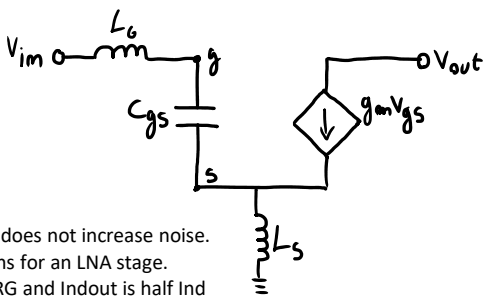


The dual alternative to the previous case.
Problem: Resistance RG by itself makes F higher than 2 (3dB).
Advantages: If Qin is higher than 1 F is lower than in the previous case.

- Degemerated commmon source (DCS)

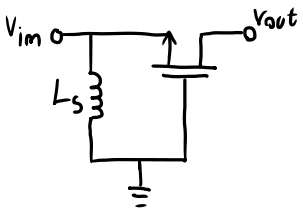


$$Z_{im} = \frac{g_m L_S}{C_{gs}} + s(L_G + L_S) + \frac{1}{sC_{gs}}$$



Inductive feedback creates a resistive part in Zin without any resistance, so it does not increase noise.
A good gain-noise trade off is achieved. One of the most popular solutions for an LNA stage.
Advantages Better than CSSR because Re(Zin) does not generates noise like RG and Indout is half Ind

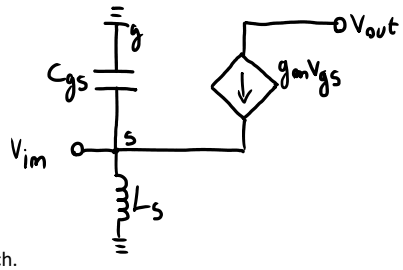
- Common Gate (CG)



$$Z_{im} = \frac{1}{sC_{gs} + g_m + 1/sL_s}$$

If we have ressonance:

$$Z_{im} = \frac{1}{g_m}$$

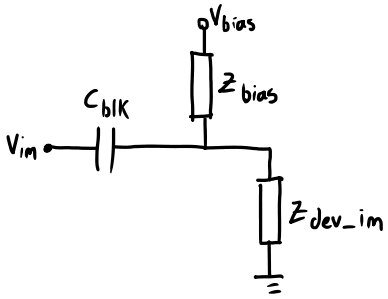


Problem: The main problem with CG is that F value is conditioned by input match.

Biasing networks

An ideal bias circuit should apply DC bias to the device without affecting the signals. Sometimes in single-ended circuits the bias is voltage type.

Input side device bias:

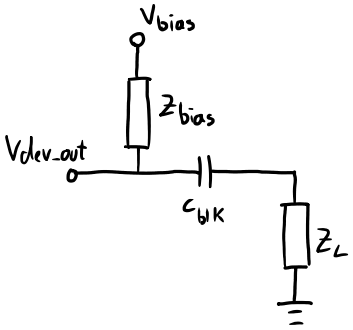


- C_{blk} → DC blocking capacitor (AC Coupling)

  $|Z_{C_{blk}}| \ll |Z_{dev\_im}|$ to allow AC to pass

- $|Z_{bias}| \gg |Z_{dev\_im}|$ → the input current goes all to the device

Output side device bias:



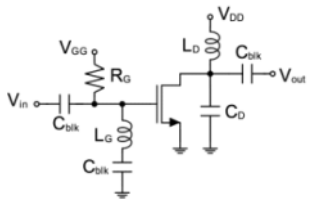
- Similar to before
  - $|Z_{C_{blk}}| \ll |Z_L|$ To only block DC
  - $|Z_{bias}| \gg |Z_L|$ So we don't sink the signal

Z_{bias} Implementation

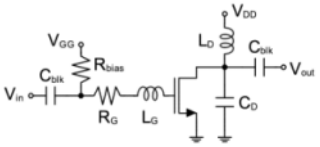
If the bias is applied to a MOSFET gate, a simple resistance can be used because there is no DC current. Alternatively, if the input network has already an inductor between bias node and ground it can be used to apply the bias, avoiding the extra resistance.
If the bias is applied to a MOSFET drain or source, the resistor is avoided not to cause power loss, so the inductor is preferable.

Topologies w/ the bias network

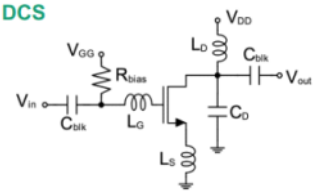
CSPR



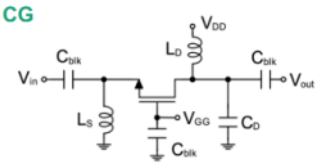
CSSR



DCS



CG



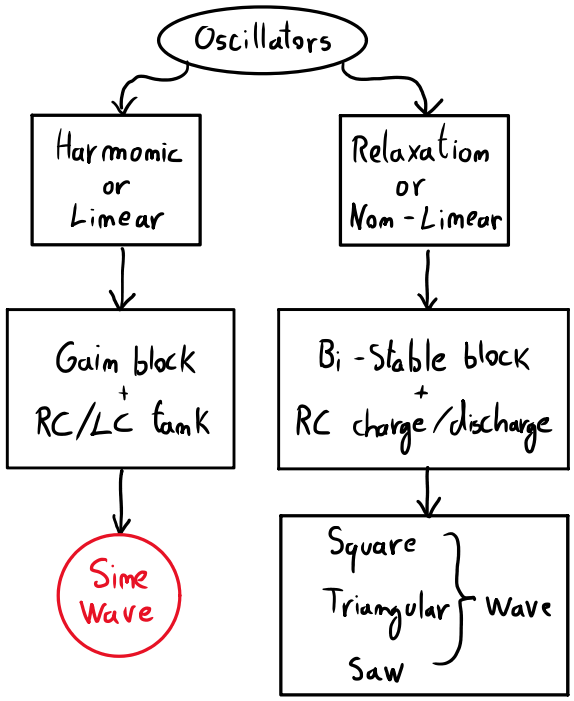
Sinusoidal Oscillators

Introduction

Basic Concepts

- Oscillator: Circuit that produces a time variant signal using only static power supply.
- Working Behavior: Interaction between a passive circuit and one or more active elements.
- Nonlinear Behavior: Necessary to stabilize oscillation magnitude in the steady-state regime.
- Steady-state Regime: Time period that starts when all varying electrical signals became periodic.
- Start-up Regime: The initial time interval where electrical signals increase their magnitude from zero up to the steady-state regime start point.

Classification



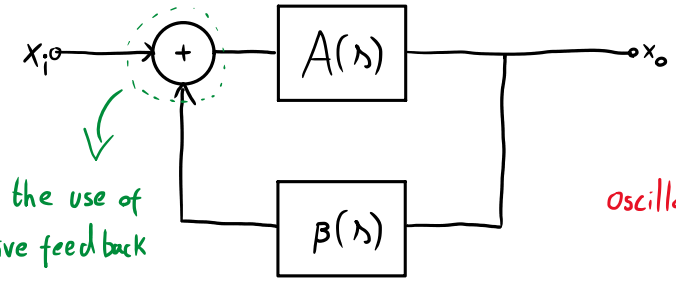
Characterization:

- Oscillation Frequency (f0): Output signal fundamental frequency.
- Harmonic Distortion: Output signal harmonic distortion.
- Output Power: Power delivered to the load at f0 frequency.
- Efficiency: The ratio between the output power and the power supplied by the bias source(s).
- Spurious: Output components at frequencies that are not harmonically related to f0 oscillation frequency
- Amplitude Moise: Random perturbation of the output signal amplitude.
- Phase Noise: Random perturbation of the output signal phase.
- Start-up Time: Time the oscillator needs to reach the steady-state regime.
- Settling Time: Time the oscillator takes to change between two steady-state frequencies.
- Pulling: Oscillation frequency change due to a load impedance variation.
- Pushing: Oscillation frequency change due to supply voltage variation.

Oscillator Theory

Oscillation Condition

a) Feedback Method:



Transfer Function:

$$\frac{X_o}{X_i} = \frac{A(s)}{1 - A(s)\beta(s)}$$

Barkausem Criteria: It oscillates if

Oscillation Condition $\rightsquigarrow A(s)\beta(s) = 1$

Some aspects about Feedback Method:

• Assuming the analysis in made in the frequency domain, the advantage is that CAD is more suitable for simulating jω frequency response rather than Laplace s-domain transfer functions. Also, oscillating frequency hand-made calculation is ease to perform if s=jω is used in the oscillation condition.

• The main drawback is that at high-frequencies it can be difficult to identify A and B blocks, because individual components also present internal feedback which cannot be neglected.

• Usually, there is no loop node that can be used for open-loop gain analysis without causing loading effects influence.

b) Root Locus Method

Oscillation Condition $\rightsquigarrow$ A pair of complex poles located im the imaginary axis

Some aspects about Root Locus Method:

Implies the calculation of the circuit poles!
For high frequency circuits this is a difficult task because:

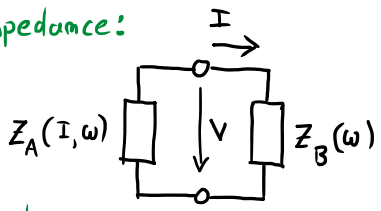
• Many capacitances => high order circuit => high number of poles whose location expressions are complicated.

• If distributed behavior => infinite number of poles.

• CAD is more suitable to simulate jw frequency response rather than Laplace s-domain transfer functions.

c) Matrix Analysis Method: One-Port Impedance/Admittance Case

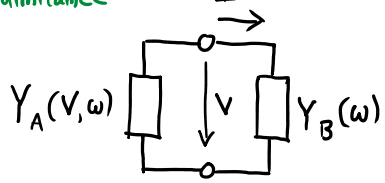
- Impedance:



If $Z_B(\omega) \gg 0$, I higher harmonics ≈ 0 => $I \approx$ sine

Oscillation Condition $\rightsquigarrow Z_A(I,\omega) + Z_B(\omega) = 0$

- Admittance



If $Y_B(\omega) \gg 0$, V higher harmonics ≈ 0 => $V \approx$ sine

Oscillation Condition $\rightsquigarrow Y_A(V,\omega) + Y_B(\omega) = 0$

Some aspects about One-Port Method:

• On the steady-state regime an oscillator has usually, voltage V or current I with approximately sinusoidal waveform. This depends on how the passive network (B block) filters the electrical quantities.

• In accordance the nonlinearity should be characterized in terms of the sinusoidal waveform amplitude (V or I).

• The correct oscillation condition to use is the one that is close to the real oscillator behavior, i.e., the impedances condition if I is to be sinusoidal, or the admittances condition if V is to be sinusoidal.

Start-Up Condition

The start-up regime is mandatory for an oscillator to reach the expected working behavior in the steady-state regime.

The start of the oscillations begin in the small-signal regime because the oscillation magnitude is very low. This means that the start-up can be studied for small-signal condition.

Oscillator circuits must be unstable in small signal level, so, a small perturbation like noise or a power-up transient are enough to start the oscillating behavior.

During the start-up regime the signal increases its amplitude which reduces gain of the oscillator non-linear A block, up to the instant when the frequency and the signal magnitude satisfy the oscillation condition. At this instant, the steady-state regime starts.

During start-up the instantaneous oscillating frequency can be slightly different from steady-state frequency.

a) Feedback Method:

Start-Up condition ⇝ In small signal: $|A(s)\beta(s)|>1$ for $A(s)\beta(s) \neq 0°$

→ The system is unstable and the oscillations build-up

Besides all the pros and cons already mentioned, this method only analyzes global stability => Does not predict start-up frequency. But it is an exact stability/instability analysis (excluding loading effects influence)

b) Root Locus Method:

Start-Up condition ⇝ A pair of conjugate poles in the right-half complex plane

Besides all the disadvantages already mentioned for this method when applied to high-frequency circuits.

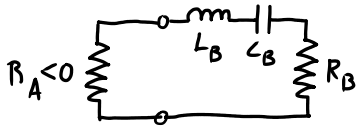
The location of the poles change from small-signal regime up to steady-state. In small signal the poles must lie on the RHP, with the compression of the non-linear block gain, they move to the final position in the imaginary axis.

It is also an exact stability/instability analysis.

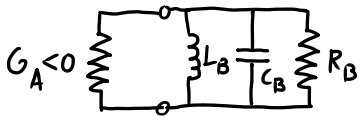
c) Matrix Analysis Method: One-Port Impedance/Admittance Case

Start-Up condition:

- Impedance: $\mathrm{Re}[Z_A+Z_B(\omega)]<0$ and $\mathrm{Im}[Z_A+Z_B(\omega)]\approx 0$



- Admittance: $\mathrm{Re}[Y_A+Y_B(\omega)]<0$ and $\mathrm{Im}[Y_A+Y_B(\omega)]\approx 0$



Advantage: Start-up frequency estimation.

Disadvantage: Approximated method because a real oscillator is neither a series nor parallel true RLC circuit.

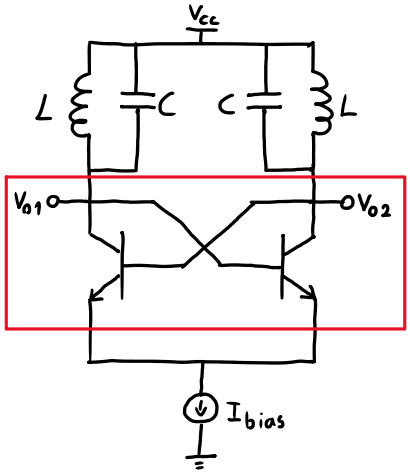
Oscillators and VCOs circuits

a) Differential LC Oscillator

Advantages:

Differential outputs → better for silicon IC

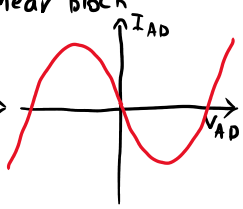
Current source bias → better for silicon IC



→ Cross-Coupled differencial pair

Nonlinear block

N shape →

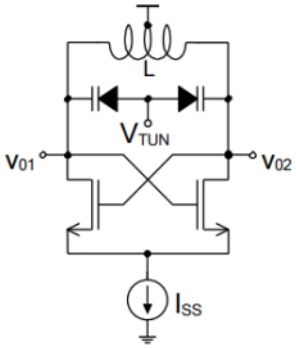


For small signals → $Y_A = -g_m/2$

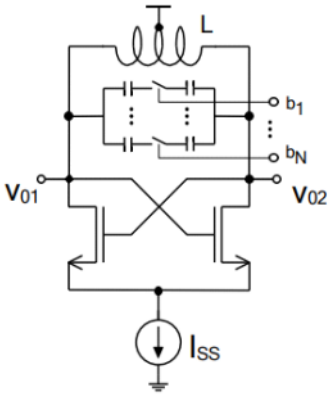
Voltage V_{AD} ≈ sine wave => $Y_A + Y_B = 0$

Frequency Controlled Oscillators

- Only reference frequency oscillators work on a single frequency. Examples are clock generators or crystal oscillators.
- In telecommunications applications oscillators must be tuned for different frequencies.
- The frequency tuning is made by changing the LC tank resonant frequency.
- Changing the L value is not an easy task, especially when a spiral inductor is used.
- The most popular option is to change the C value.
- A voltage-controlled oscillator, VCO, is an oscillator with continuous tuning function of a control voltage. Varactors based on MOS device are used.
- A discrete controlled oscillator, DCO, is an oscillator with discrete tuning function of a control digital word. Switched capacitor banks are used.



VCO



DCO

Phase-Noise

The output signal of a noiseless sinusoidal oscillator is given by: $V_{out}(t) = V_0 \cos(\omega_0 t + \varphi)$

If noise exists at the oscillator output, it will modulate both amplitude and phase that became random signals: $V_{out}(t) = A(t) \cos(\omega_0 t + \varphi(t))$

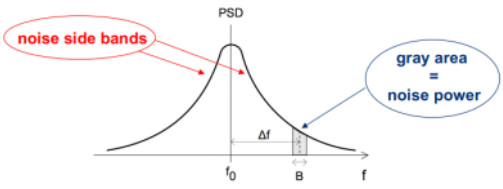
The noise that appears in every electrical quantities of the oscillator is generated by the noise sources inside the circuit.

An amplitude stabilizing mechanism is present in all oscillators and it tends to reduce amplitude modulation.

Phase noise, the phase modulation caused by noise, is more important in telecommunication systems than amplitude noise which is the amplitude modulation caused by noise.

Several methods are available to analyze oscillators noise, from simple to more sophisticated ones. Usually, different assumptions are made during the problem approach.

Oscillator phase-noise output power spectral density



Phase-noise Power (P_N) is the obtained by integrating its PSD in a certain bandwidth B.

A oscillator phase-noise FOM is defined as (P_N/B)/P_S for a given distance Δf away from f_0. This way the noise is for 1Hz bandwidth. P_S is the signal power.

If the side bands are symmetric the upper one use is usual. Units are dBc/Hz (c=carrier) for a given distance Δf, for example, -100dBc @ 1MHz.

Monolithic Integrated Frequency Mixers

Introduction

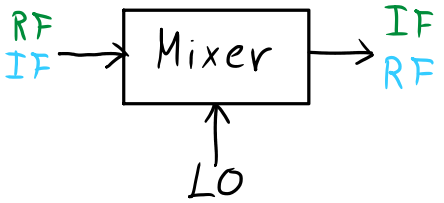
Basic Concepts

- Mixer: Circuit whose function is to perform the frequency translation of a given signal.

- Working Behavior:
  - Frequency translation requires a nonlinear or a time variant circuit behavior.
  - Only a circuit like this will produce new frequencies at the output that do not exist at its inputs.
  - If the required translation is to a multiple frequency of the input, it is only necessary to use one of the output signal harmonics.
  - However, if the required frequency is not harmonically related with the input, an auxiliary oscillator must be used (local oscillator – LO) to perform the translation.

- Applications
  - In the Emitter (up-conversion): frequency translation from a low frequency to a high frequency.
    Ex: From baseband (BB) or low frequency signal IF1 (intermediate frequency - IF) to a higher frequency, like transmission frequency (RF) or IF2.
  - In the Receiver (down-conversion): frequency translation from high frequency to a low frequency.
    Ex: From RF or IF1 to a lower frequency signal, IF2 or BB.

Characterization



Down Conversion

Up Conversion

- Conversion Gain:
  Power (or voltage, current, etc) gain between input and output signals. The power gain can be transducer, available or power gains.

$$G_{Emitter} = \frac{P_{RF}(f_{RF})}{P_{IF}(f_{IF})} \qquad G_{Receiver} = \frac{P_{IF}(f_{IF})}{P_{RF}(f_{RF})}$$

- Ports Matching:
  Some of the mixer ports, RF, LO or IF, can be matched to a certain impedance value. In this case their matching is usually characterized with reflection coefficient.

- Conversion Gain Compression:
  Like in an amplifier, 1dB compression point for the conversion gain can be obtained. It is desirable that the mixer does not reach that point in order to avoid the output signal amplitude distortion. Third-order intermodulation distortion also applies. In systems with phase modulated signal GC phase distortion must be analyzed too.

- Conversion Efficiency:
  Ratio between the mixer output power (P_{IF}) and the total power (AC+DC) supplied to the mixer ($P_{RF}+P_{LO}+P_{DC}$).

- LO Power:
  Required local oscillator power, P_{LO}, at LO port. The higher its value, more difficult the LO design will be.

- Noise Factor:
  Ratio between the input SNR (at input frequency) to the output SNR (at output frequency).

$$NF_{Receiver} = \frac{SNR_{RF}}{SNR_{IF}} \qquad NF_{Emitter} = \frac{SNR_{IF}}{SNR_{RF}}$$

- LO-IF Isolation:
  Is the LO attenuation when it reaches the IF port. This value must be as high as possible.

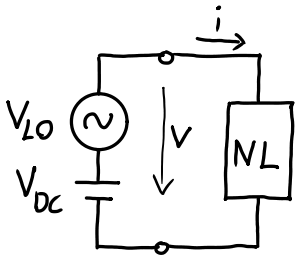
$$LO\text{-}IF = \frac{P_{LO}(f_{LO})}{P_{IF}(f_{LO})}$$

- LO-RF Isolation:
  Is the LO attenuation when it reaches the RF port. This value must be as high as possible.

$$LO\text{-}RF = \frac{P_{LO}(f_{LO})}{P_{RF}(f_{LO})}$$

Mixers Theory

One-Tone Excitation



NL is $i = f(v)$ type and memoryless described by:

$i(v) = av + bv^2$ where $v = V_{DC} + V_{LO}\cos(\omega_{LO}t)$

So

$$i = I_{DC} + I_{LO}\cos(\omega_{LO}t) + I_{2LO}\cos(2\omega_{LO}t)$$

Where

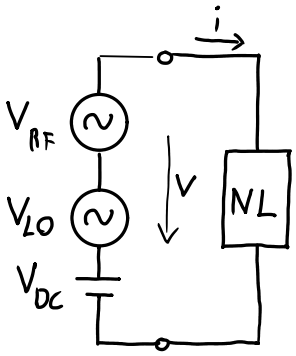
DC Component $I_{DC} = aV_{DC} + bV_{DC}^2 + \frac{b}{2}V_{LO}^2$

1st Harmonic Component $I_{LO} = aV_{LO} + 2bV_{DC}V_{LO}$

2nd Harmonic Component $I_{2LO} = \frac{b}{2}V_{LO}^2$

All depend on V_{LO}!

Two-Tone Excitation



Example 1: Both RF and LO are strong signals

Same as before but: $v = V_{DC} + V_{LO}\cos(\omega_{LO}t) + V_{RF}\cos(\omega_{RF}t)$

$$\Rightarrow i = I_{DC} + I_{LO}\cos(\omega_{LO}t) + I_{2LO}\cos(2\omega_{LO}t) + I_{RF}\cos(\omega_{RF}t) + I_{2RF}\cos(2\omega_{RF}t) + I_{RF-LO}\cos[(\omega_{RF}-\omega_{LO})t] + I_{RF+LO}\cos[(\omega_{RF}+\omega_{LO})t]$$

DC Component $I_{DC} = aV_{DC} + bV_{DC}^2 + \frac{b}{2}V_{LO}^2 + \frac{b}{2}V_{RF}^2$

2nd Harmonic Component $\begin{cases} I_{2LO} = \frac{b}{2}V_{LO}^2 \\ I_{2RF} = \frac{b}{2}V_{RF}^2 \end{cases}$

1st Harmonic Component $\begin{cases} I_{LO} = aV_{LO} + 2bV_{DC}V_{LO} \\ I_{RF} = aV_{RF} + 2bV_{DC}V_{RF} \end{cases}$

2nd Order Intermodulation Products $I_{RF-LO} = I_{RF+LO} = bV_{LO}V_{RF}$

Example 2: One strong and one weak signal

$\begin{cases} i = f(v) \\ v = V_{strong} + v_{weak} \end{cases}$ $\Rightarrow$ Use Taylor Series $\Rightarrow i \approx f(V_{strong}) + \left.\frac{df(v)}{dv}\right|_{V_{strong}} \cdot v_{weak}$

$V_{strong} = V_{DC} + V_{LO}$

$v_{weak} = V_{RF}$

$i(V_{strong}) = I_{DC} + I_{LO}\cos(\omega_{LO}t) + I_{2LO}\cos(2\omega_{LO}t)$ → One Tone!

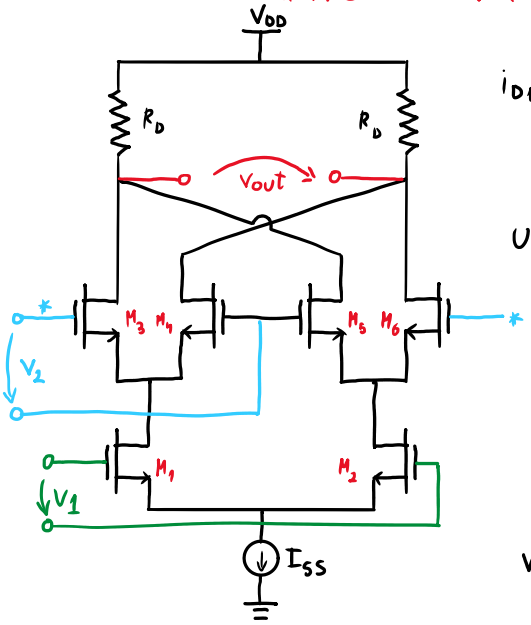
$+$

$$\left.\frac{df(v)}{dv}\right|_{V_{strong}} \cdot v_{weak} = \left(a + 2b\cdot[V_{DC} + V_{LO}\cos(\omega_{LO}t)]\right)V_{RF}\cos(\omega_{RF}t)$$

Note LO ± RF mixing products have the same value as in last example

Mixers Circuits

Double-Balanced Mixer (Gilbert Cell)



$$V_{out} = R_D(i_{D4} + i_{D6} - i_{D3} - i_{D5})$$

$$i_{D1,2} \approx \frac{I_{SS}}{2} \pm V_1\sqrt{\frac{KI_{SS}}{2}}$$

$$i_{D3,4} \approx \frac{i_{D1}}{2} \pm V_1\sqrt{\frac{Ki_{D1}}{2}}$$

↳ M_1 acts as a current source for the pair $M_{3,4}$

$$i_{D5,6} \approx \frac{i_{D2}}{2} \pm V_1\sqrt{\frac{Ki_{D2}}{2}}$$

↳ M_2 acts as a current source for the pair $M_{5,6}$

Using $\sqrt{1+x} \approx 1 + \frac{x}{2}$ when $x \approx 0$ we can write:

$$i_{D3,4} = \left(\frac{I_{SS}}{4} + \frac{V_1}{2}\sqrt{\frac{KI_{SS}}{2}}\right) \pm V_2\sqrt{\frac{KI_{SS}}{2}}\left(1 + V_1\sqrt{\frac{K}{2I_{SS}}}\right)$$

$$i_{D5,6} = \left(\frac{I_{SS}}{4} - \frac{V_1}{2}\sqrt{\frac{KI_{SS}}{2}}\right) \mp V_2\sqrt{\frac{KI_{SS}}{2}}\left(1 - V_1\sqrt{\frac{K}{2I_{SS}}}\right)$$

$$V_{out} = -\sqrt{2}\,kR_D V_1 V_2$$

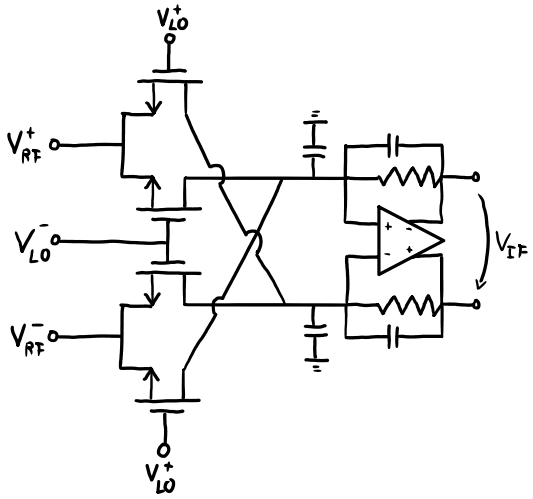
If $V_1 = V_{RF}\cos(\omega_{RF}t)$

$V_2 = V_{LO}\cos(\omega_{LO}t)$ $\Rightarrow$ $G_C = \frac{V_{out}}{V_1} = \frac{kR_D}{\sqrt{2}}V_{LO}$

$V_{out} = V_{IF}\cos(\omega_{IF}t)$

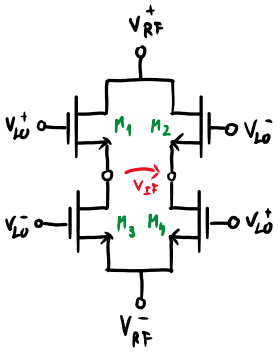
Comments:
- 4 quadrants multiplier.
- Good isolation between v1 or v2 to vout.
- High GC, low NF.
- Linearity is higher than the single-balanced case.
- Differential accesses.

Switch Mode Mixer



Comments:
- Transistors work as switches.
- Reactive components filter unwanted high order mixing products.
- Highly linear but high NF.
- OPAMP can be a low frequency component.

Switching Passive Mixer

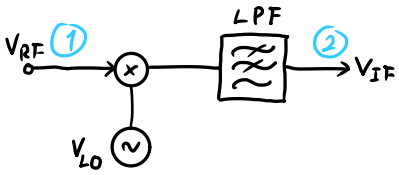


Comments:
- Low conversion gain.
- High linearity.
- Mi switching => High level LO

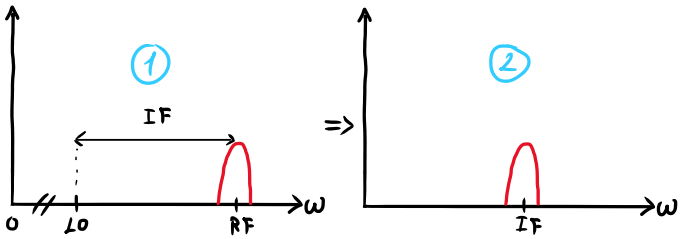
Radio Architectures

Heterodyne Receiver

This architecture uses one or more intermediate frequencies (IF). Invented by Armstrong in 1918. It is still the most used topology in transceivers.

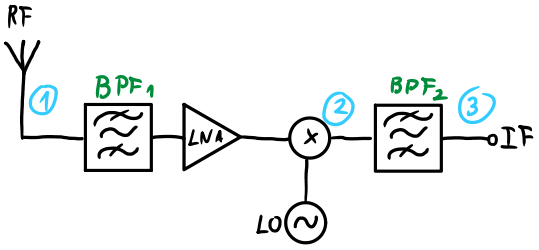


$$V_{IF}(t) = \frac{A_{RF} A_{LO}}{2} \cos\left[(\omega_{RF} - \omega_{LO})t\right]$$



Down Conversion

In reality the signal received by the antenna has not just the desired signal. Lots of systems coexist in the open air. Also, in modern telecommunication systems several channels exist in the same service band. So, a more realistic receiver needs filters.



BPF_1 - Preselect filter / band filter

BPF_2 - Channel select filter

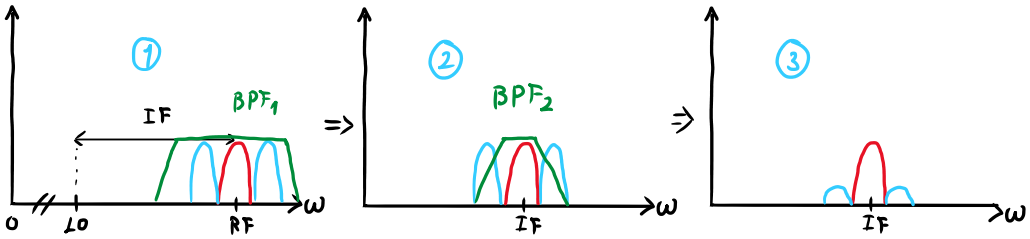
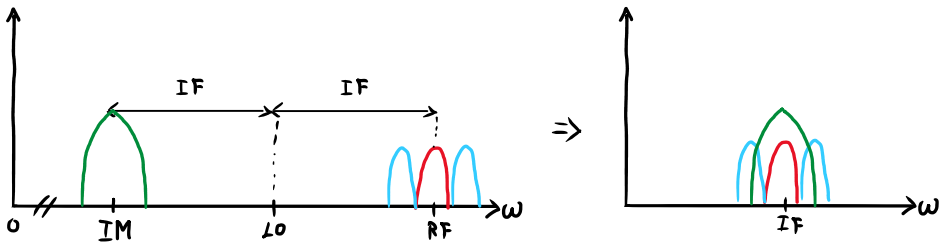
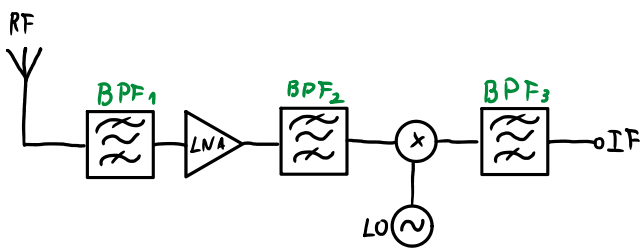


Image Frequency

The image frequency (IM) is down converted to IF like the desired frequency (RF) and corrupts it.

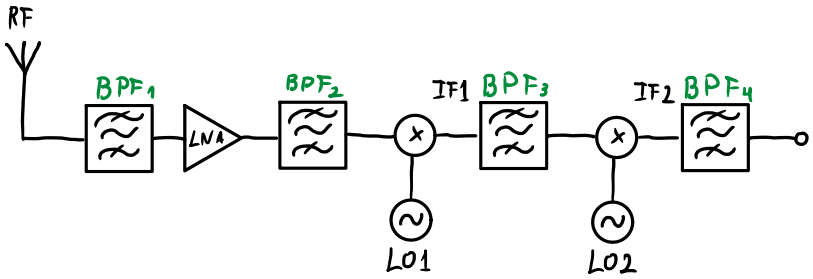


Although BPF_1 minimizes IM signal at the RF mixer input, it can be further reduced with image reject filter, BPF_2. Additionally, it filters LNA output noise at IM frequency, improving receiver NF



Dual IF

The image rejection selectivity trade-off can be improved if a dual IF topology is used. A higher IF_1 can be used simplifying BPF_2, and the channel selection is improved by BPF_4 at lower frequencies. Sometimes IF_2 is equal to 0 and BPF_4 becomes LPF_4.



Note that in the second downconversion the image problem also appears but, because the frequency is lower and BPF_3 reject it, it is not so severe.

BPF_1 is usually off-chip. Sometimes is the duplexer used in full-duplex transceivers.

BPF_2 is also off-chip because of its high Q value. Usually, a SAW or ceramic filter is used. But these filters are 50 matched, so the LNA output must be 50 matched. This means that buffers must be used increasing power consumption. The cost is also higher.

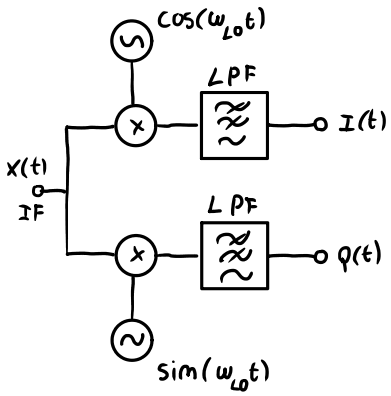
Off-chip filters are less expensive if standard frequencies are chosen. Example, FM radio, RF=[88,108]MHz, IF=10.7MHz (crystal filter), AM radio, RF=[540,1600]kHz, IF=455kHz.

Channel tuning is usually made by changing LO_1 frequency. In this case LO_2 frequency has a fixed value.

Signal Demodulation

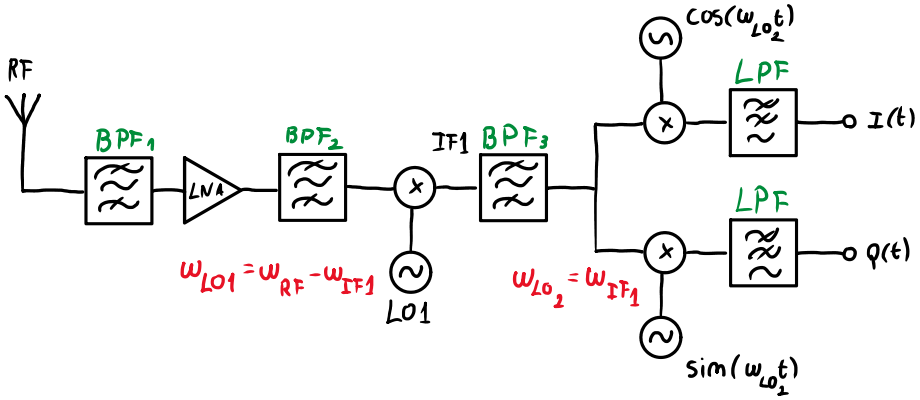
If the lower IF stage produces a slow enough signal for the ADC, then the signal demodulation (recover the BB information signal) can be done in the digital domain (DSP). Another option is to make the demodulation in the analog domain. Depending on the modulation type, this can be done if the last IF frequency is enough low or zero.

Modern communication systems use digital modulation techniques. This means that instead of a single BB signal, there are two BB signals, I(t) and Q(t). Demodulation has to be done by mixing with two signals in quadrature



Typical Architecture

For digital IQ modulation a typical receiver is:

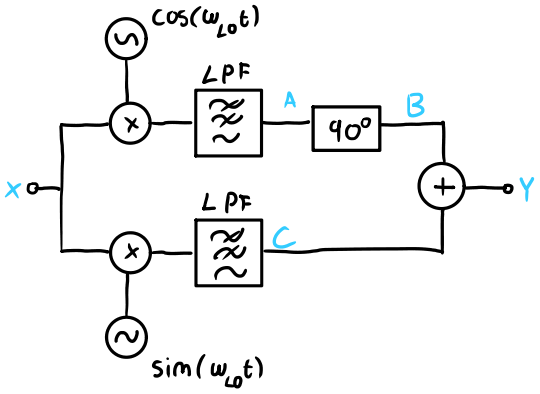


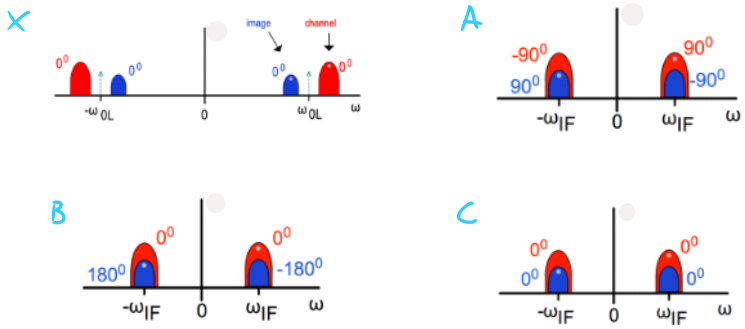
A channel pre-selection can be made by BPF_3 if IF_1 is fixed, which means that LO_1 must tune the channel frequency. LPF perform the final channel selection. IF_1 is lower than RF which is better to reduce quadrature and phase impairments at LO_2.

Image Cancelation Architectures

To avoid the need for an image reject filter, other suppression methods can be used. For example, canceling the image at the output by adding two signals that have it with opposite signs.

> Hartley



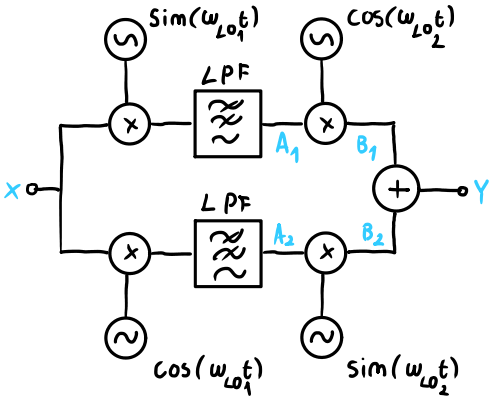


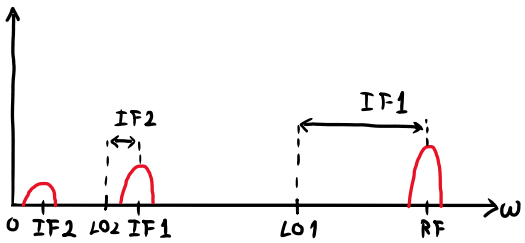
B + C = Y

⇓

No image, only the channel

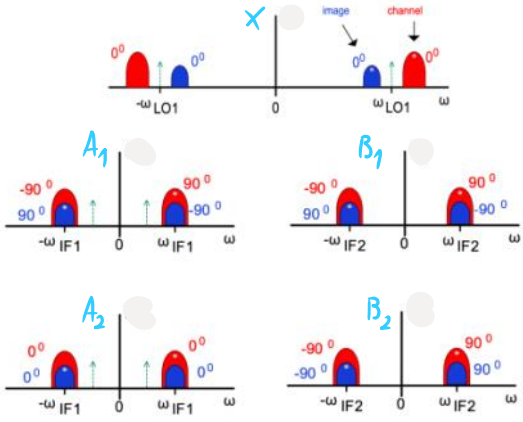
> Weaver





Output $Y = B_1 + B_2$ has no image

Works by frequency plamming : $\omega_{IF_2} = \omega_{RF} - \omega_{LO1} - \omega_{LO2}$



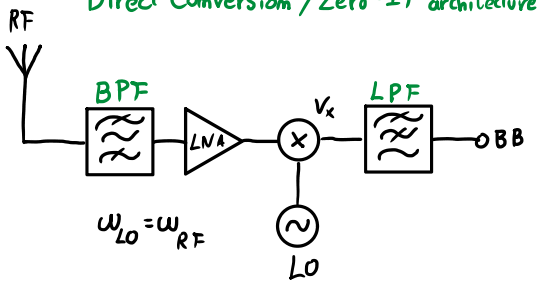
It is assumed that out off band components are filtered.

Same cancelation principle as Hartley but phase-shifter is replaced by 2nd quadrature stage.

Homodyne Receiver

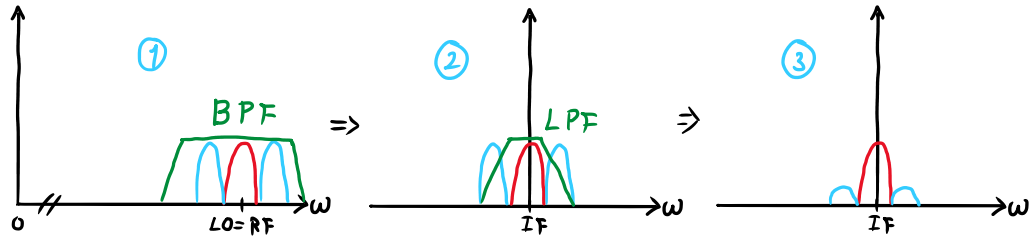
It is an architecture that down converts the RF signal directly to base-band (BB). This means that $\omega_{LO}=\omega_{RF}$ and $\omega_{IF}=0$.

Direct Conversion / Zero-IF architecture



The major advantage is that a homodyne receiver doesn't suffer from the image frequency problem.

No image-rejection needed.



Also, IF filters are not needed.

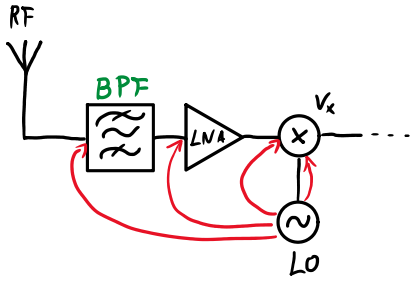
Channel select low-pass filter is usually active.

Between this filter, the ADC and a possible amplifier between them, a good noise-linearity-power trade-off must exist.

DC Offsets

If at the RF and LO mixer inputs the same interference signal appears, on the mixer IF port a DC component is generated. This component can saturate the following stages and ruin the receiver performance.

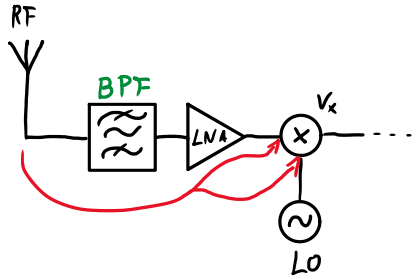
Self-Mixing



Due to poor mixer LO-RF isolation, the LO signal is successively reflected in the RF chain ports mismatches and mixes with himself. Substrate coupling can also be responsible for this effect.

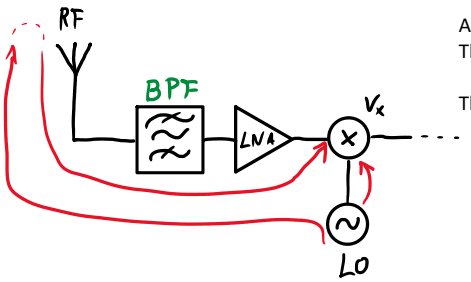
This same effect is less severe in heterodyne because LO frequency is lower than LO=RF frequency.

Strong Interference



A strong interference signal can cross the RF chain, leak to the LO port and mix with itself.

Time Varying Offset

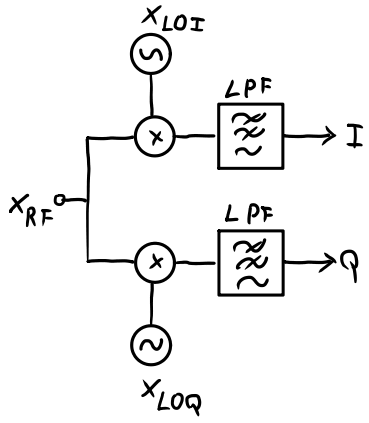


Any leak from the LO to the antenna can reflect in a moving object and produces a time varying self-mixing effect. This is worst if the receiver is moving.

This produces a low-frequency time varying offset which is very difficult to distinguish from the desired signal.

I/Q Mismatch

Errors in the amplitude and quadrature relations of the quadrature demodulator will affect I(t) and Q(t) BB signals. Suppose that the amplitude and quadrature mismatch between the oscillators are ε and θ, respectively.



$$x_{RF} = I_x(t)\cos(\omega_{RF}t) + Q_x(t)\sin(\omega_{RF}t)$$

$$x_{LOI} = \left(1+\frac{\varepsilon}{2}\right)\cos\left(\omega_{RF}t + \frac{\theta}{2}\right)$$

$$x_{LOQ} = \left(1-\frac{\varepsilon}{2}\right)\cos\left(\omega_{RF}t - \frac{\theta}{2}\right)$$

$\omega_{LO} = \omega_{RF}$

$$I = \left(1+\frac{\varepsilon}{2}\right)\left[\frac{I_x(t)}{2}\cos\left(\frac{\theta}{2}\right) - \frac{Q_x(t)}{2}\sin\left(\frac{\theta}{2}\right)\right]$$

$$Q = \left(1-\frac{\varepsilon}{2}\right)\left[\frac{I_x(t)}{2}\sin\left(\frac{\theta}{2}\right) - \frac{Q_x(t)}{2}\cos\left(\frac{\theta}{2}\right)\right]$$

Amplitude only: $\varepsilon \neq 0$ and $\theta = 0$

$$I = \frac{I_x(t)}{2}\left(1+\frac{\varepsilon}{2}\right) \qquad Q = \frac{I_x(t)}{2}\left(1-\frac{\varepsilon}{2}\right)$$

Only a gain factor that affects the BB signal

Not severe

Phase only: $\varepsilon = 0$ and $\theta = 0$

$$I = \frac{I_x(t)}{2}\cos\left(\frac{\theta}{2}\right) - \frac{Q_x(t)}{2}\sin\left(\frac{\theta}{2}\right)$$

$$Q = \frac{I_x(t)}{2}\sin\left(\frac{\theta}{2}\right) - \frac{Q_x(t)}{2}\cos\left(\frac{\theta}{2}\right)$$

I has a fraction of Q

Q has a fraction of I

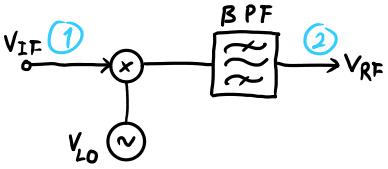
This degrades the signals

Typical required values for mismatch are below 1dB for amplitude and 5 degrees for quadrature.

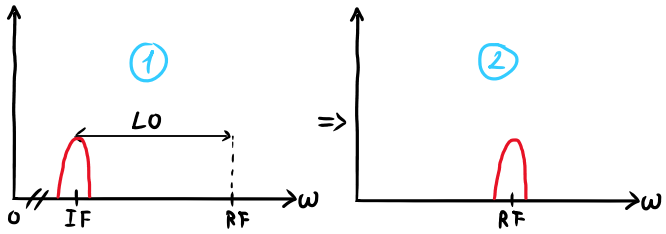
In this aspect the heterodyne with quadrature demodulator is better due the lower LO2 frequency of the second quadrature demodulator.

Heterodyne Transmitter

It is an architecture that uses one or more intermediate frequencies (IF).



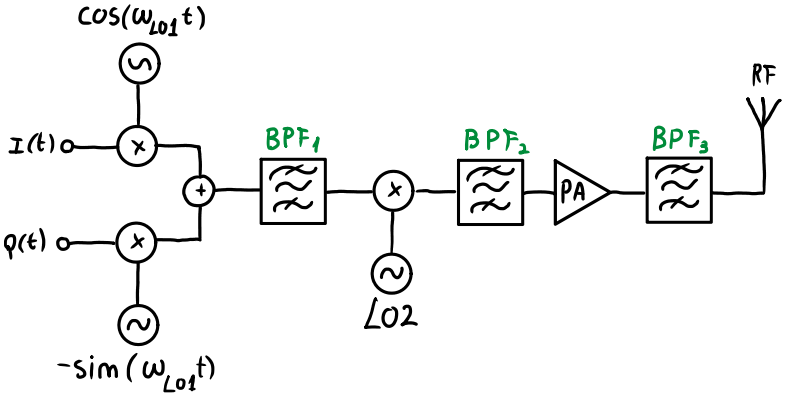
$$V_{RF}(t) = \frac{A_{IF}A_{LO}}{2}\cos\left[(\omega_{IF}+\omega_{LO})t\right]$$



Up Conversion

Typical Architecture

For digital IQ modulation a typical emitter is:



- BPF_1 and BPF_2 necessary to filter mixers outputs.

- BPF_3 eventually needed to filter PA output.

Advantages

➢ PA output frequency is far away from LO frequency => Less oscillator pulling.

➢ Quadrature stage at IF => Less sensitive to mismatch.

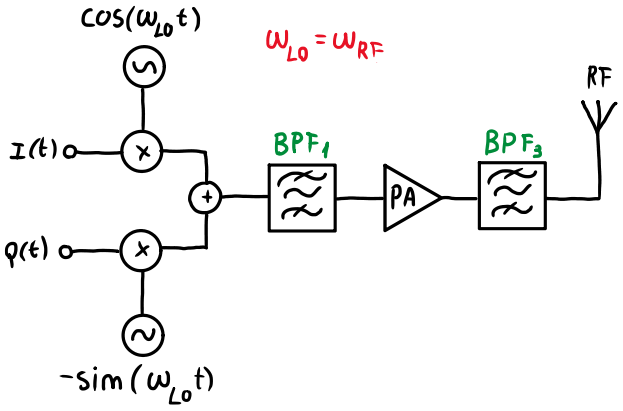
Disadvantages

➢ More complicated circuit.

➢ More filters.

Homodyne Transmitter

For digital IQ modulation a typical emitter is:



Advantages
- ➢ Simple circuit.
- ➢ Lower chip area required than the heterodyne.

Disadvantages
- ➢ PA interferes with LO at the same frequency due to poor isolation => oscillator pulling.
- ➢ LO leakage.
- ➢ RF I/Q mismatch.

High-Efficiency RF Power Amplifiers

Introduction

Mobile Phones

GSM ⇒ UMTS ⇒ LTE

CDMAone ⇒ CDMA2000 ⇒ LTE

2G 3G 4G

Wireless Internet Access

IEEE ⇒ IEEE ⇒ IEEE

802.11b ⇒ 802.11agm ⇒ 802.16m

WiFi WiFi WiMax

Modern systems transmit more information => Higher data rate.

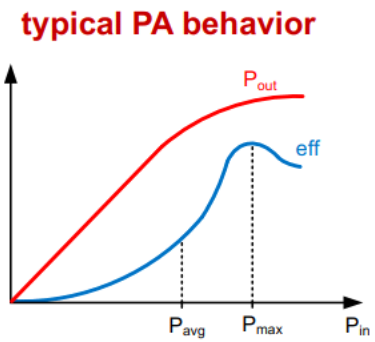
Spectrum is scarse and need to be used efficiently => More sophisticated signals with both phase and amplitude modulation (OFDM, M-QAM).

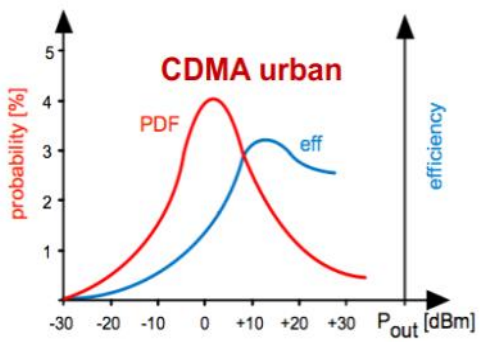
It is difficult to build linear and energy efficient power amplifiers (PA) for signals that do not have a constant envelope (amplitude modulation) => New solutions have to be studied.

Usually, the RF signals to amplify have instantaneous power peaks much higher than the signal average power.

$$\eta_{avg} = \frac{\bar{P}_{out}}{\bar{P}_{DC}} = \frac{\int_{P_{min}}^{P_{Max}} p \cdot PDF(p)\, dp}{\int_{P_{min}}^{P_{Max}} \frac{p}{\eta(p)} \cdot PDF(p)\, dp}$$

Because the peaks cannot be distorted, the PA is almost all the time working well bellow its maximum efficiency.





Peak to Average Power Ratio $PAPR = \frac{P_{peak}}{P_{average}}$

Called Crest Factor if magnitudes are used

System	Modulation	PAPR [dB]
GSM	GMSK	0
GPRS	GMSK	0
EDGE	8PSK	3.2
UMTS	HPSK	3.5 - 7
CDMAone	QPSK	5.5 - 12
CDMA2000	HPSK	4 - 9
802.11b	QPSK	3
802.11a/g	OFDM	6 - 17

Power Amplifiers Requirements

- High output power
- High efficiency
- Stability
- Linearity
- Power Gain

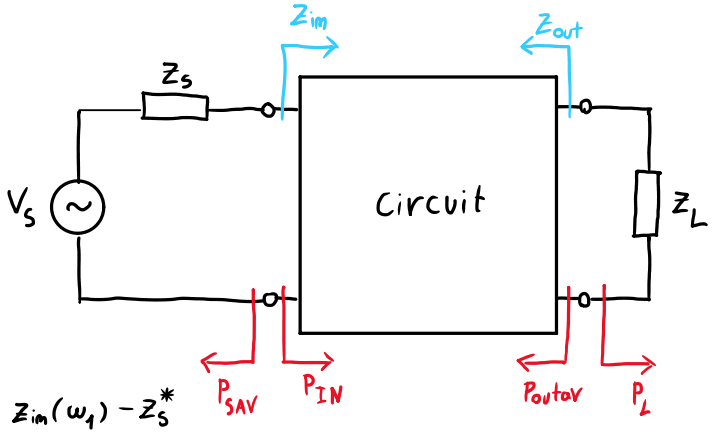
Characterization

Power Gains

Operating Power Gain – $G_P = \frac{P_L(\omega_1)}{P_{IN}(\omega_1)}$

Available Power Gain – $G_A = \frac{P_{outSAV}(\omega_1)}{P_{SAV}(\omega_1)}$

Transducer Power Gain – $G_T = \frac{P_L(\omega_1)}{P_{SAV}(\omega_1)}$



Input matching $Z_{im} = \frac{V_{im}(\omega_1)}{I_{im}(\omega_1)} \longrightarrow \rho_{im} = \frac{Z_{im}(\omega_1) - Z_S^*}{Z_{im}(\omega_1) + Z_S}$

Efficiency

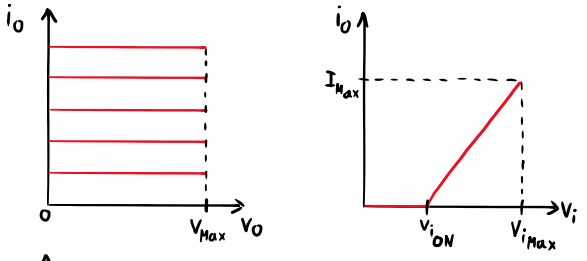
Output efficiency: $\eta = \frac{P_L}{P_{DC}}$

Power Added Efficiency (PAE): $PAE = \frac{P_L - P_{IN}}{P_{DC}}$ => Is important when the gain is not high

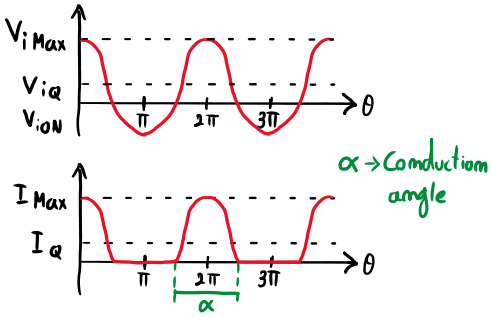
Classical Classes

Conventional RF classes: A to C

Transistor (device) acts as a voltage controlled current source $i_O(v_i)$.
The output circuit is tuned at f_0 => v_L is sinusoidal.
The behavior depends on the input voltage v_i and device $i_O(v_i, v_O)$ characteristics.



Note:
- BJT: $i_O = i_C$, $V_O = V_{CE}$, $V_i = V_{BE}$
- Mos: $i_O = i_D$, $V_O = V_{DS}$, $V_i = V_{GS}$



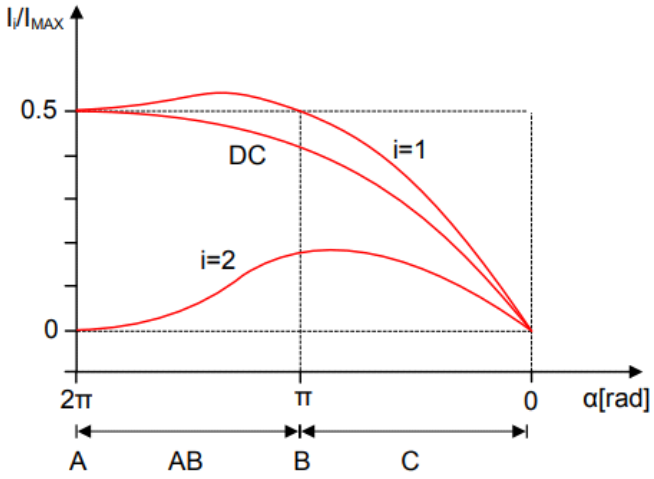
Class	α [rad]	IQ/IMAX
A	2π	0.5
AB	] π,2π [	] 0,0.5 [
B	π	0
C	] 0, π [	0

Fourier analysis of I_o waveform

$$I_{DC} = I_o = \frac{I_{Max}}{2\pi} \cdot \frac{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cdot\cos\left(\frac{\alpha}{2}\right)}{1-\cos\left(\frac{\alpha}{2}\right)}$$

$$I_1 = \frac{I_{Max}}{2\pi} \cdot \frac{\alpha - \sin(\alpha)}{1-\cos\left(\frac{\alpha}{2}\right)}$$

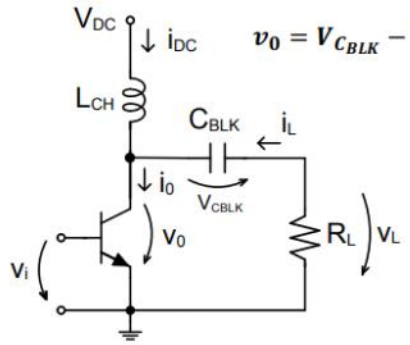
DC and fund. are enough for calculations



Notes on V_o

- Depends on device ouput current I_o and device load impedance
- $V_{Mim} = 0$ for ideal device (Also called Knee Voltage)

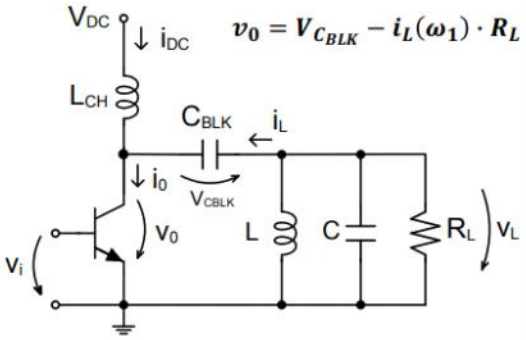
wideband output circuit



$v_0 = V_{C_{BLK}} - i_L \cdot R_L$

- i_0 has DC and AC parts
- i_L has only AC part because of C_{BLK}
- v_0 DC part is equal to V_{DC} because of L_{CH}
- i_{DC} has only DC part because ωL_{CH}>>
  $\Rightarrow i_{DC} = i_0$ DC part.
- V_{Cblk} has only DC part because ωC_{BLK}>>
  $\Rightarrow v_0 = v_L$ AC part = $-i_L R_L$ AC part

tuned output circuit



$v_0 = V_{C_{BLK}} - i_L(\omega_1) \cdot R_L$

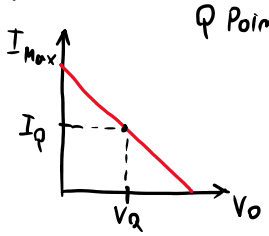
- i_0 has DC and AC parts
- i_L has only AC part because of C_{BLK}
- v_0 DC part is equal to V_{DC} because of L_{CH}
- i_{DC} has only DC part because ωL_{CH}>>
  $\Rightarrow i_{DC} = i_0$ DC part.
- V_{Cblk} has only DC part because ωC_{BLK}>>
  $\Rightarrow v_0 = v_L$ AC part = $-i_L(\omega_1)R_L \Rightarrow$ sinewave

Note: Following study of classical classes assume tuned output circuits

Class A:

$\alpha = 2\pi$

Q Point: $I_Q = \frac{I_{Max}}{2} = I_1$ $\quad V_Q = \frac{V_{Max}}{2}$

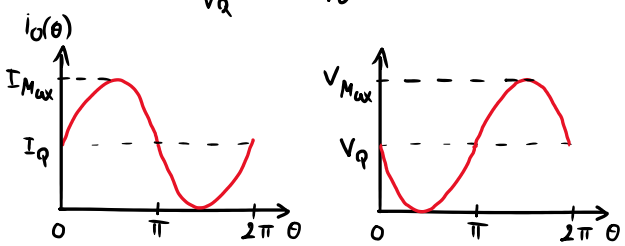


$R_{LA} = \frac{V_{Max}}{I_{Max}}$ $\quad R_L = \frac{V_Q}{I_1} = R_{LA}$ $\quad P_L = \frac{1}{2} R_L I_1^2 = P_{LA}$

$P_{DC} = I_Q V_Q = 2P_{LA}$ $\quad P_{Diss} = P_{DC} - P_L = P_{LA}$ $\quad \eta = \frac{P_L}{P_{DC}} = 50\%$

Advantages:
- Io current without distortion (theoretical) => Unnecessary output filter.
- High gain.

Disadvantages:
- Low efficiency.
- With null input signal => PDISS=PDC

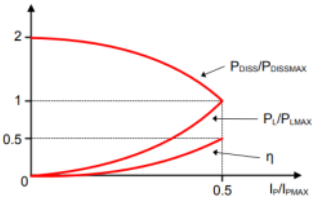


For less than max excursion:

$$\frac{P_L}{P_{L\,Max}} = 4\left(\frac{I_P}{I_{MAX}}\right)^2$$

$$\eta = 2\left(\frac{I_P}{I_{MAX}}\right)^2$$

$$\frac{P_{Diss}}{P_{Diss\,Max}} = 2 - 4\left(\frac{I_P}{I_{MAX}}\right)^2$$



Class B :

Q Point :

$I_Q = 0$

$V_Q = \frac{V_{Max}}{2}$

Harmonics :

$I_0 = I_{DC} = \frac{I_{Max}}{\pi}$

$I_1 = \frac{I_{Max}}{2}$

Tuned Load

$R_L = R_{LA}$ } Equal to A

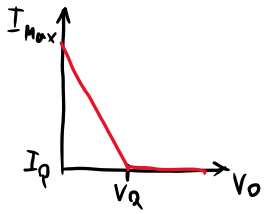
$P_L = P_{LA}$ }

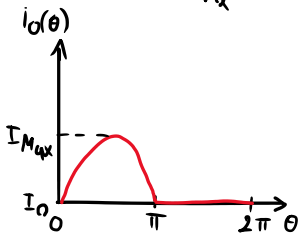
$P_{DC} = \frac{2}{\pi} P_{LA}$ }

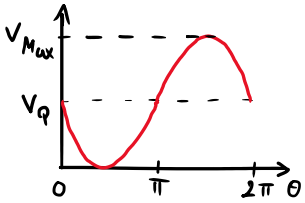
$P_{DISS} = \frac{4-\pi}{\pi} P_{LA}$ } Less than A

$\eta = 78.5\%$ Better than A

$\alpha = \pi$





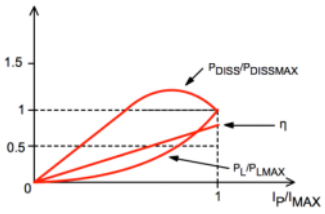


For less than max excursion:

$$\frac{P_{DISS}}{P_{DISS\,Max}} = \frac{\pi}{4-\pi}\left[\frac{4}{\pi}\left(\frac{I_P}{I_{Max}}\right) - \left(\frac{I_P}{I_{Max}}\right)^2\right]$$

$$\frac{P_L}{P_{L\,Max}} = 4\left(\frac{I_P}{I_{MAX}}\right)^2$$

$$\eta = \frac{\pi}{4}\left(\frac{I_P}{I_{MAX}}\right)^2$$



Advantages:
- Higher efficiency than class A.
- With null input signal => PDISS=0.

Disadvantages:
- io current has distortion => output filter is necessary.
- Lower gain than class A.

Class AB :

$\pi < \alpha < 2\pi$

Q Point :

$I_Q = I_{Max} \cdot \frac{\cos(\frac{\alpha}{2})}{1-\cos(\frac{\alpha}{2})}$

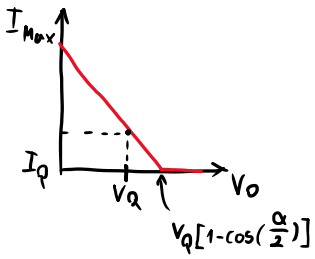
$V_Q = \frac{V_{Max}}{2}$

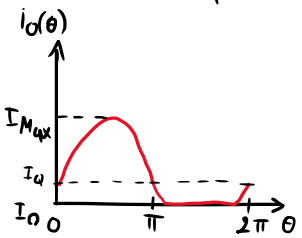
Harmonics :

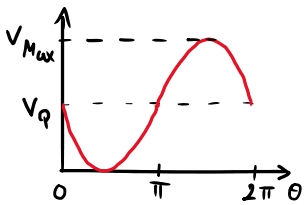
$I_0 = \frac{I_{Max}}{2\pi} \cdot \frac{2\,\mathrm{sim}(\frac{\alpha}{2}) - \alpha\cos(\frac{\alpha}{2})}{1-\cos(\frac{\alpha}{2})}$

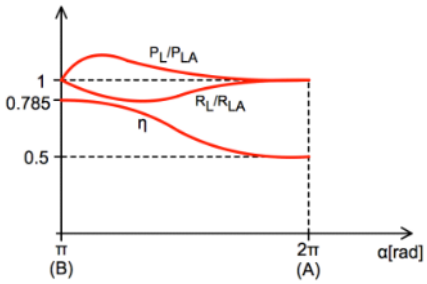
$I_1 = \frac{I_{Max}}{2\pi} \cdot \frac{\alpha - \mathrm{sim}(\alpha)}{1-\cos(\frac{\alpha}{2})}$

$\eta = \frac{1}{2} \cdot \left[\frac{\alpha - \mathrm{sim}(\alpha)}{2\,\mathrm{sim}(\frac{\alpha}{2}) - \alpha\cos(\frac{\alpha}{2})}\right]$









Advantages:
- Higher efficiency than class A.
- Less distortion than class B.

Disadvantages:
- io current has distortion => output filter is necessary.
- Lower gain than class A.

Class C:

$0 < \alpha < \pi$

Q Point :

$I_Q = 0$

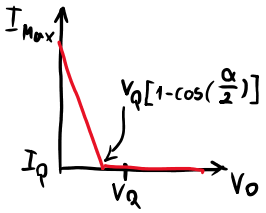
$V_Q = \frac{V_{Max}}{2}$

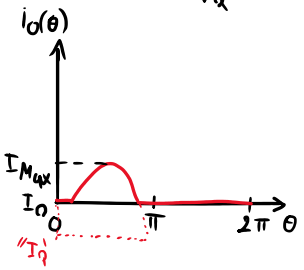
Harmonics :

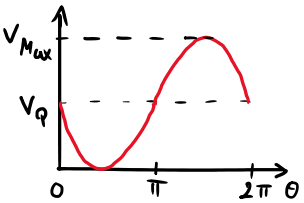
$I_0 = \frac{I_{Max}}{2\pi} \cdot \frac{2\,\mathrm{sim}(\frac{\alpha}{2}) - \alpha\cos(\frac{\alpha}{2})}{1-\cos(\frac{\alpha}{2})}$

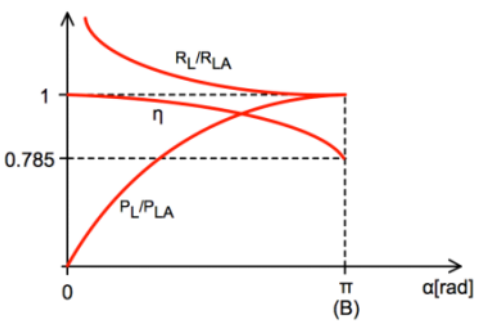
$I_1 = \frac{I_{Max}}{2\pi} \cdot \frac{\alpha - \mathrm{sim}(\alpha)}{1-\cos(\frac{\alpha}{2})}$

$\eta = \frac{1}{2} \cdot \left[\frac{\alpha - \mathrm{sim}(\alpha)}{2\,\mathrm{sim}(\frac{\alpha}{2}) - \alpha\cos(\frac{\alpha}{2})}\right]$





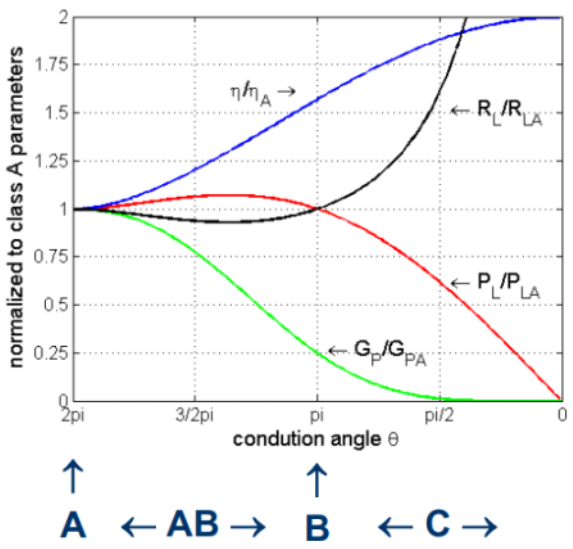




Advantages:
- Higher efficiency than class B.

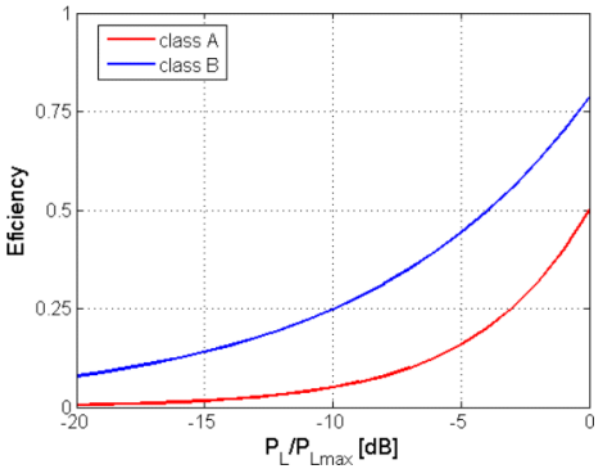
Disadvantages:
- io current has distortion => output filter is necessary.
- Lower gain than class B.

For maximum excursion:



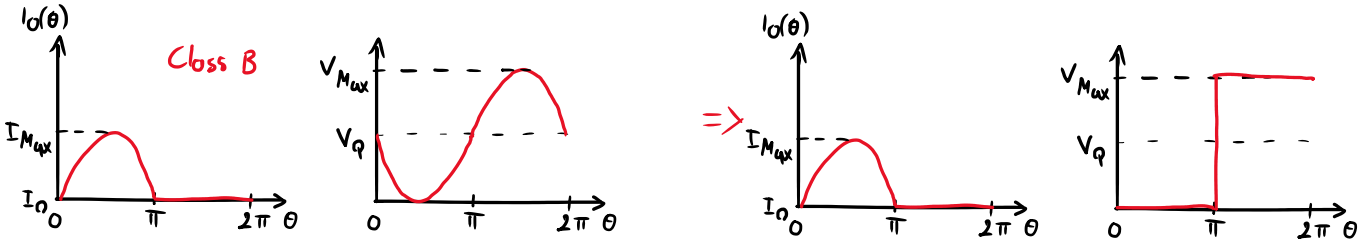
Class A and B under output power back off

Not maximum excursion



Saturated Classes

Squaring class B voltage:



By minimizing $p(\theta) = v_o(\theta) \cdot i_o(\theta)$ the efficiency is increased $\Rightarrow P_{diss} = 0 \Rightarrow \eta = 100\%$. With ideal components

odd harmonics are added to $v_o(\theta)$ and $i_o(\theta)$ is equal to class B

We need to synthesize the load: $m = 1 \rightarrow Z_L(\omega_0) = \frac{4}{\pi} R_{LA}$

m even $\rightarrow Z_L(m\omega_0) = 0 \rightarrow i_o$ has even harmonics but v_o has not

m odd $\rightarrow Z_L(m\omega_0) = \infty \rightarrow v_o$ has odd harmonics but i_o has not

Class F: To synthesize $Z_L(\omega)$ an infinite number of resonators is used

Ideal Resonator $\rightarrow Z_{tank}(\omega) = \begin{cases} \infty & \text{if } \omega = \omega_{res} \\ 0 & \text{if } \omega \neq \omega_{res} \end{cases} \Rightarrow$ $I_{o\,Max} = \pi \frac{P_L}{V_{DC}}$, $V_{o\,Max} = 2 V_{DC}$

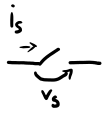
Class F with maximally flat voltage: To synthesize $Z_L(\omega)$ a finite number of resonators is used

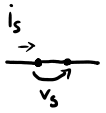
Inverse Class F: The i_o wave is squared!

Switched Classes

Introduction:

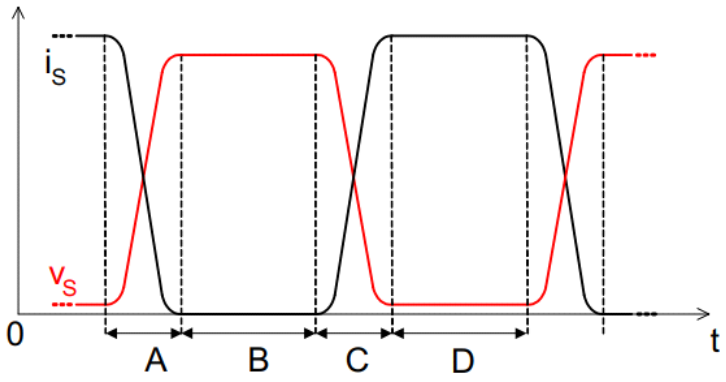
Transistor as an ideal switch:

OFF  $\begin{cases} i_s = 0 \\ v_s \neq 0 \end{cases} \Rightarrow P = v_s \cdot i_s = 0$

ON  $\begin{cases} i_s \neq 0 \\ v_s = 0 \end{cases} \Rightarrow P = v_s \cdot i_s = 0$

Remarks:
- Necessary to minimize time periods with both $i_S>0$ and $v_S>0$.
- In the OFF state the transistor is close to ideal switch.
- In the ON state the transistor has R_{ON} triode resistance => losses.
- The change between states is not instantaneous due to transistor capacitive effects => losses.

Im reality



Time Intervals

B - Not critical ($i_s \approx 0$)

D - Important ($v_s \neq 0$)

A/C - Very Important ($v_s \neq 0$ and $i_s \neq 0$)

At low freqs A and C are negligible

- Current Mode Class D (CMCD)

Is ZVS -> Zero Voltage Switch : the transistor turns ON when the voltage is zero

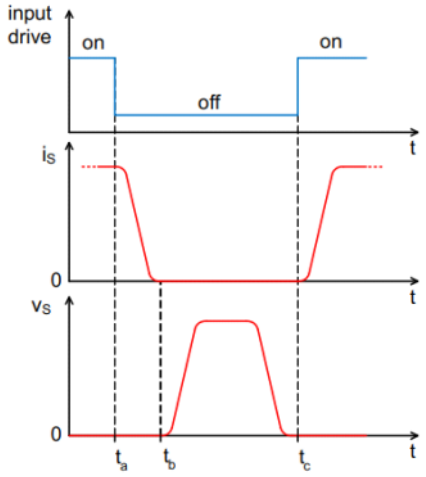
If a class is non-ZVS, when the switch turns on, the transistor output capacitance will be discharged through R_{DSon}. These losses are proportional to frequency, so non-ZVS PAs are not suitable for high-frequencies applications.

- Class E

The class development is based on the inevitable fact that transistors take some time to change between ON and OFF states.

The idea is to shape the waveforms in A and C time intervals to minimize simultaneous coexistence.

This is done by proper choice of transistor load impedance.
The problem is analyzed and solved in both time and frequency domain.



ON => OFF

V_S must increase only after i_S current becomes ≈ 0

OFF => ON

a) V_S is zero (ZVS)

b) V_S derivative is zero (ZSVS)